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DC bias elimination for Dual-Active-Bridge DC/DC converters using TMS320F28335

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Abstract

This paper proposes an novel simple anti-bias modulation technique for single phase Dual-Active-Bridge DC/DC converters. When a pulsating load occurs, the control efforts of the controller lead to sudden changes in the phase shift. In turn, this cause a momentary unbalance in the positive and negative volt-second product of the transformer. As a consequence, DC bias in the transformer current appears and takes some time to vanish. By some small changes in the setting of the pulse-width-modulation modules of the digital-signal-processor, the bias can be completely eliminated. Theoretical analysis and experimental results show that, it takes only a half of one switching period to remove the bias caused by a pulsating load change without the need of a high sampling speed or any complicated measurements or feedback.

Keywords: *Dual-Active-Bridge DC/DC converter; DC bias elimination; transformer saturation; phase shift modulation; TMS320F28335*

Symbols

Symbols	Units	Description
B	T	Flux density
ψ	radian	Phase shift angle
λ	Weber	Volt-second product
ω_s	V	switching frequency in rad/s
A_c	m^2	Cross-section are of the core
N_1	Turns	Number of turns of pri. winding
L_k	H	leakage inductance
σ	p.u.	Inductance ratio

Abbreviations

DAB	Dual-Active-Bridge
ePWM	enhanced Pulse Width Modulation
SPS	Single Phase Shift
TBCTR	Timer-based Counter
TBPHS	Timer-based Phase Shift
TBPRD	Timer-based Period
CMPx	Compare x (x = ∈ A, B)

Tóm tắt

Bài báo này đề xuất một phương pháp đơn giản để loại bỏ thành phần quá độ một chiều trong đáp ứng dòng điện của bộ biến đổi lưỡng cầu một pha. Khi tải thay đổi đột ngột với biên độ lớn, bộ điều khiển thường cố gắng tác động nhanh để ổn định dòng điện (điện áp) tải. Biến điều khiển (góc dịch pha) do đó cần được thay đổi với số gia lớn. Tuy nhiên, việc này gây ra sự mất cân bằng trong việc từ hóa máy biến áp do thành phần một chiều xuất hiện trong dòng điện và cần một khoảng thời gian để suy giảm về không. Trong bài báo này, một kỹ thuật đơn giản dựa trên việc tinh chỉnh cài đặt các mô-đun điều chế độ rộng xung của vi điều khiển TMS320F28335 được trình bày. Nhờ có kỹ thuật đó, thành phần quá độ một chiều được loại bỏ hoàn toàn trong chỉ trong một nửa chu kỳ đóng cắt mà không cần thêm cảm biến hay tăng tốc độ lấy mẫu. Hiệu quả của kỹ thuật đề xuất được kiểm chứng thông qua phân tích toán học và thực nghiệm.

1. Introduction

As already discussed in many articles [1, 2], Dual-Active-Bridge (DAB) converters have many interesting features, such as: isolated and bidirectional power transmission, inherited soft-switching, high power density, high efficiency, etc. Among those, simple control structure is a very important characteristics that make DAB converter an attractive topology for industry applications. Conventionally, handling the power flow of a DAB converter requires only one phase shift variable. This method, which is called the Single-Phase-Shift (SPS) technique, uses 180 degree conduction mode in both inverters, and shifts the output voltage of one inverter prior or posterior that of the other.

Although very simple and robust, SPS modulation also has some drawbacks, such as narrow soft-switching area, high circulating current, limited voltage range, DC-bias in transformer current, etc. Many advanced control method have been pub-

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lished to solve these problems, such as Enhanced-Phase-Shift (EPS) [3, 4, 5], Dual-Phase-Shift (DPS) [6, 7, 8] and Triple-Phase-Shift (TPS) [9, 10, 11]. Those techniques are proposed mainly to deal with extending the soft-switching area of the converter. However, there are few researches on dealing with the latter one, DC-bias in transformer current.

The DC bias may be caused due to several reasons such as: unbalance gate signal due to different propagation delay time of drivers, unequal voltage drop or different rise/fall time of switching devices, pulsating load change, etc. [12, 13, 14, 15, 16, 17]. The DC-bias appears in the transformer (and the external inductor, if any) can make the devices saturated. The DC-bias also introduces unwanted additional dissipation on the magnetic device as heat due to the increment of core loss. It can also causes excessive current stress on switching devices. Therefore, it is necessary to eliminate the DC-bias.

Some causes of the DC-bias such as unbalance gate signal, unequal power electronic device parameters, etc. can be avoided by hardware optimization, for example, by choosing the devices from the same production lots, reducing the number of driving stages (e.g., using isolated gate driver instead of normal gate driver and digital isolators), etc. Nevertheless, hardware optimization cannot help to remove the DC-bias caused by pulsating load changes. When a pulsating load occurs, the control efforts of the controller lead to sudden changes in the phase shift. In turn, this cause a momentary unbalance in the positive and negative volt-second products of the transformer. As a consequence, DC bias in the transformer current appears and takes some time to vanish that, beside the aforementioned effects, slows down the dynamics of the overall system.

A blocking capacitor may be the easiest way to block the DC component of transformer currents, however, at the price of additional volume, cost and loss to the system. Ortiz *et.al.* in [12] summarized some active/passive methods to suppress the bias based on actual flux measurement. Nevertheless, external circuits must be used that adds complexity and reduces the system reliability. In contrary, the approaches proposed in [13, 14, 15] aiming to deal with the DC-bias caused by pulsating load change were based on advancing the modulation pattern or control algorithm. The switching period was discretized into sub-periods in [13] to allow fine-tuning of the switching pattern. However, this requires very high sampling frequency that may not applicable in many cases. The technique proposed in [14] was dedicated for EPS-modulated DAB converter but also applicable for SPS-modulated one. However, it requires to modify the modulation of all legs to deal with the bias. Moreover, there is a division in the calculation of new modulation parameters that leads to the possibility of a division-by-zero error when voltages at both sides are equal. The anti-bias strategy reported in [15] seems simpler than the two previous techniques. Although it can suppress the DC-bias in a half of one switching period, it needs a sampling speed of two times faster than the switching frequency.

From another aspect, all proposed modulation algorithms must be undertaken in a processor platform. The effect of anti-bias techniques depends strongly on the updating mechanism of the modulators of the processor. However, that issue is not discussed in all of the aforementioned articles. Let us take the prevailing 32-bit DSP TMS320F28335 from Texas Instrument for instance, when the phase shift modulation mode is implemented for its PWM modules, any updates of modulation

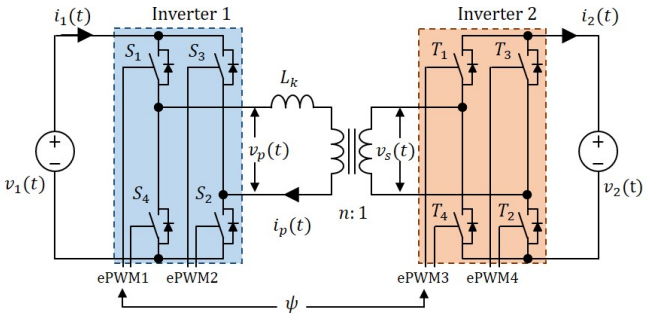

Figure 1: Dual-Active-Bridge DC/DC converter.

parameters are written to the corresponding registers at the end of current switching period [18]. All changes made in prior of that instant have no effects. Consequently, some of the above techniques may no longer be applicable.

This paper proposes a simple technique to eliminate the DC-bias caused by pulsating load change. The approach is to balance the volt-second product (i.e. the flux linkage) of the transformer. The control platform utilized in this research is a TMS320F28335 DSP. The relationship between the DC-bias creation and the updating mechanism of PWM modules of the DSP is revealed and used for modifying the modulation pattern appropriately. As will be seen later, the bias is suppressed in just a half of one switching cycle like that reported in [15]. However, the sampling speed required by the technique proposed in this paper is just as high as the switching frequency. Furthermore, while in [15], all four modulators need to be modified to suppress the bias, only one module is adjusting here. No complicated calculation is carried out. The proposed algorithm can thus be deployed as an additional post-processing procedure before passing to the PWM modules.

This paper is structured as follows: Section 2 describes the SPS implementation and operation on TMS320F28335, from that, equations to model the flux linkage are derived; Section 3 explains the creation of DC-bias when pulsating load change occurs; method to eliminate the bias is proposed in Section 4; experimental results are presented in Section 5 to confirm the validity the method; and finally, pros. and cons. of the proposed technique are provided in Section 6.

2. Phase shift modulation of DAB converter on TMS320F28335 DSP

A typical DAB converter has two inverters and one high frequency transformer located in the middle for isolation and voltage matching as depicted in Figure 1. There are four MOSFET (or IGBT) legs switching at the same frequency. In order to handle the power flow in the converter, the most popular and simplest method is the single-phase-shift (SPS) technique which controls the phase displacement between output voltages of the two inverters. A positive phase displacement implies a forward power transmission and vice versa.

As mentioned before, a 32-bit DSP TMS320F28335 from Texas Instrument is utilized to control the operation of the system. Four enhanced pulse-width-modulation (ePWM) modules are used, ePWM1 and ePWM2 are dedicated for two legs of Inverter 1 (the sending side); and ePWM3 and ePWM4 are for Inverter 2 (the receiving side). They are configured for

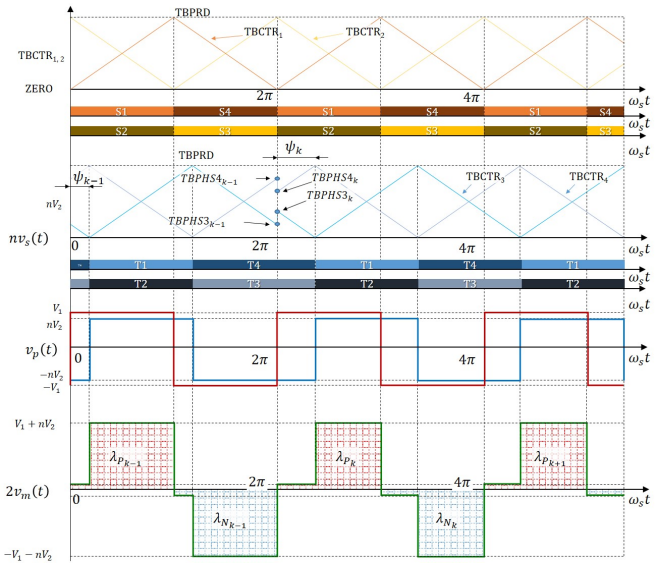

Figure 2: Theoretical waveforms by the original SPS modulation.

functioning the SPS modulation as follows :

- Up-down counting mode;
- Complementary outputs for each leg;
- ePWM1 is the master module, the other three are slaves;
- Phase shift modulation mode is enable;
- Synchronization is at TBCTR1 = zero;
- ePWM2 and ePWM4 are 180 degrees shifted from ePWM1 and ePWM3, respectively;
- ePWM3 is ψ degrees shifted from ePWM1.
- All set at ZRO (TBCTRx = ZERO) and clear at PRD (TBCTRx = TBPRD), where TBCTRx (x $\in [1,4]$) is the counting register of the corresponding ePWM module; and TBPRD is the period register (same for all modules);
- "Do nothing" at TBCTRx = CMPAx and TBCTRx = CMPBx events, where CMPAx and CMPBx (x $\in [1,4]$) are the counting-compare registers A and B of the corresponding ePWM module.

Table 1 summaries the setting of the Action-Qualifier Output registers of all ePWM modules. Because of this setting, output voltages $v_p(t)$ and $v_s(t)$ of the two inverters have the two-level, square-wave forms and ψ degrees shifted from each other; where ψ is the phase shift variable. Figure 2 demonstrates the theoretical waveforms of two consecutive switching periods.
Considers the simplified, primary-referred equivalent circuit diagram depicted in Fig. 3, where L_{k_1} and L_{k_2} are the total inductance of the primary and secondary sides, respectively; L_m is the magnetizing inductance. The magnetizing inductance

Table 1: Configuration of Action-Qualifier Output x registers.

Event	Setting	Note
TBCTRx = CAU	Do nothing	TBCTRx = CMPA at counting up
TBCTRx = CAD	Do nothing	TBCTRx = CMPA at counting down
TBCTRx = CBU	Do nothing	TBCTRx = CMPB at counting up
TBCTRx = CBD	Do nothing	TBCTRx = CMPB at counting down
TBCTRx = ZRO	Set	TBCTRx = zero
TBCTRx = PRD	Clear	TBCTRx = period

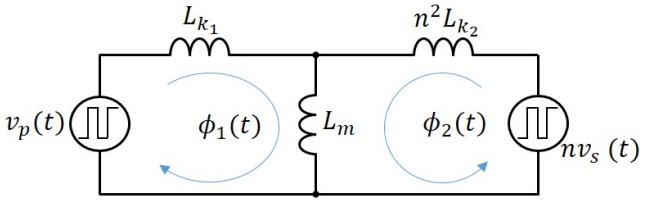

Figure 3: Equivalent circuit diagram.

L_m is usually omitted because it is much greater than the total series inductance referred to the primary side (i.e. $L_k = L_{k_1} + n^2L_{k_2}$, n is the transformer turns ratio). Here, L_m is kept in the diagram aiming to consider the voltage-second balance of the transformer.
The voltage across the magnetizing inductor can be yielded as:

$$v_m(t) = \frac{L_{k_1}}{L_{k_1}+n^2L_{k_2}}\left(\frac{n^2L_{k_2}}{L_{k_1}}v_p(t)+nv_s(t)\right) \tag{1}$$

Let σ be the ratio between the inductances:

$$\sigma = \frac{n^2L_{k_2}}{L_{k_1}}, \tag{2}$$

Since $v_m(t)$ is the derivative of the total flux linkage in the core with respect the time t, (1) can be expressed as:

$$\frac{d\lambda(t)}{dt} = v_m(t) = \frac{1}{1+\sigma}\left(\sigma v_p(t)+nv_s(t)\right) \tag{3}$$

where n is the turns ratio, $N_1 = nN_2$; N_1 and N_2 are the number of turns of the primary and secondary windings respectively. The waveform of $v_m(t)$ is illustrated in Figure 2 for the case $\sigma = 1$ (i.e. no external series inductors at both sides). Since $v_p(t)$ and $v_s(t)$ depend on the switching state of the converter, it is worth to consider each state to determine the voltage-second product in each switching half cycle.
Let ψ_{k-1} be the phase shift at the $(k-1)^th$ switching period (corresponding to the value $TBPHS3_{k-1}$ of the phase shift register TBPHS3):

$$TBPHS3_{k-1} = \frac{\psi_{k-1}}{\pi} \times TBPRD3$$

From (3) and Fig. 2, the positive and negative volt-second products of the magnetizing inductance are determined by:

$$\begin{cases} \lambda_{P_{k-1}} = & \frac{1}{\omega_s(1+\sigma)}\left[(\sigma V_1+nV_2)\pi - 2nV_2\psi_{k-1}\right] \\ \lambda_{N_{k-1}} = & -\frac{1}{\omega_s(1+\sigma)}\left[(\sigma V_1+nV_2)\pi - 2nV_2\psi_{k-1}\right] \end{cases} \tag{4}$$

where ω_s is the switching frequency in radian-per-second. Since the summation of $\lambda_{P_{k-1}}$ and $\lambda_{N_{k-1}}$ is zero, the flux in the core is balanced. The peaks of flux density are then calculated by (5):

$$\begin{aligned} B_{pk,p_{k-1}} = -B_{pk,n_{k-1}} &= \frac{\lambda_{P_{k-1}}}{2N_1A_c} \\ &= \frac{1}{2N_1A_c\omega_s(1+\sigma)}\left[(\sigma V_1+nV_2)\pi - 2nV_2\psi_{k-1}\right] \end{aligned} \tag{5}$$

where $B_{pk,p_{k-1}}$ and $B_{pk,n_{k-1}}$ are the positive and negative peaks of flux densityat the $(k-1)^{th}$ switching cycle, respectively; and A_c is the cross section area of the magnetic core.

3. The creation of DC-bias

When a load change occurs, the controller will react to maintain the output current or voltage depending on the objective of the control system. In either cases, the phase shift ψ is likely to change. The faster dynamic of the close-loop system, the higher amplitude of the change of ψ. At the beginning of the k^{th} switching period, the new phase shift value of ψ_k is calculated then sent to the modulators and from there, corresponding PWM signals are sending to the driver system.

Obviously, the refreshing rate of ψ is the sampling frequency, however, the updating rate of the modulators of TMS320F28335 is the switching frequency. The registers of the modulators are reloaded with new values from shadow registers at the end of the current switching period [18]. The use of shadow registers allows synchronized update with the hardware. Indeed, one can use the "Immediate Load" setting to immediately write the new values to registers. However, this may lead to corruption operation or malfunction of the system due to asynchronous register modification by software. More importantly, this function is not applicable in the "Phase Shift Modulation Mode". In the phase shift mode, all register updates of slavery ePWM modules are synchronized with the master module (ePWM1) at, for example, the event of TBCTR1 = ZERO.

The synchronous update effect is illustrated in Figure 2. When TBCTR1 equals to zero at counting down ($\omega_s t = 2\pi$), all phase shift registers are reloaded with new values regardless of the writing request instants from the system. Registers TBPHS3 and TBPHS4 (the phase shift registers of ePWM3 and ePWM4, respectively) are updated with the new value of $TBPHS3_k$ and $TBPHS4_k$, respectively:

$$\begin{cases} TBPHS3_k &= \dfrac{\psi_k}{\pi} \times TBPRD3 \\ TBPHS4_k &= \left(1+\dfrac{\psi_k}{\pi}\right) \times TBPRD4 \end{cases}$$

Consequently, the volt-second products of the k^{th} switching cycle are:

$$\begin{cases} \lambda_{P_k} = & \dfrac{1}{\omega_s(1+\sigma)}\left[(\sigma V_1 + nV_2)\,\pi - 2nV_2\psi_k\right] \\ \lambda_{N_k} = & -\dfrac{1}{\omega_s(1+\sigma)}\left[(\sigma V_1 + nV_2)\,\pi - 2nV_2\psi_k\right] \end{cases} \tag{6}$$

The new peak flux densities are yielded as (7) and (8):

$$\begin{aligned} B_{pk,p_k} &= B_{pk,n_{k-1}} + \frac{\lambda_{P_k}}{N_1 A_c} \\ &= \frac{1}{2N_1 A_c \omega_s(1+\sigma)}\left[(\sigma V_1 + nV_2)\,\pi - 2nV_2\psi_{k-1} - 4nV_2\Delta\psi\right] \\ &= B_{pk,p_{k-1}} - \frac{2nV_2}{N_1 A_c \omega_s(1+\sigma)}\Delta\psi \end{aligned} \tag{7}$$

$$\begin{aligned} B_{pk,n_k} &= B_{pk,p_k} + \frac{\lambda_{N_k}}{N_1 A_c} \\ &= -\frac{1}{2N_1 A_c \omega_s(1+\sigma)}\left[(\sigma V_1 + nV_2)\,\pi - 2nV_2\psi_{k-1}\right] \\ &= B_{pk,n_{k-1}} \end{aligned} \tag{8}$$

where B_{pk,p_k} and B_{pk,n_k} are the positive and negative peaks of flux density at the k^{th} switching cycle; and $\Delta\psi$ is the deviation of the phase shift, $\Delta\psi = \psi_k - \psi_{k-1}$.

From (7) and (8), assumes that the phase shift is increasing, i.e. $\Delta\psi > 0$, the positive peak flux density decreases compared to that of the $(k-1)^{th}$ cycle, whereas the negative peak stays the same. This phenomenon is demonstrated in the $B-H$ frame in Fig. 4 for the case $\Delta\psi > 0$. Obviously, a bias in flux density is caused and the flux becomes unbalanced.

4. Flux balancing method

4.1. Approach

Let ΔB be the bias flux density, from (7), ΔB is defined as:

$$\Delta B = \frac{2nV_2}{N_1 A_c \omega_s(1+\sigma)}\Delta\psi \tag{9}$$

Notes that, flux is unbalanced when the summation of B_{max_k} and B_{min_k} is other than zero. This notation suggests an idea that, the flux in the core can be balanced by adding a half of the biased flux to both peaks of the flux density. From a geometrically view, if the B-H trajectory in Fig. 4 is shifted upward a half of the biased flux calculated by (9), the flux in the core will become balanced.

This means the positive volt-second product λ_{P_k} needs to be modified as (10) while λ_{N_k} remains unchanged.

$$\begin{aligned} \lambda^*_{P_k} &= \lambda_{P_k} + \frac{N_1 A_c \Delta B}{2} \\ &= \lambda_{P_k} + \frac{nV_2}{1+\sigma} \times \frac{\Delta\psi}{\omega_s} && \text{(10a)} \\ &= \lambda_{P_{k-1}} - \frac{nV_2}{1+\sigma} \times \frac{\Delta\psi}{\omega_s} && \text{(10b)} \\ &= \frac{1}{\omega_s(1+\sigma)}\left[(\sigma V_1 + nV_2)\,\pi - 2nV_2\psi_{k-1} - nV_2\Delta\psi\right] && \text{(10c)} \end{aligned}$$

By doing so, the positive and negative peaks of flux density becomes (11).

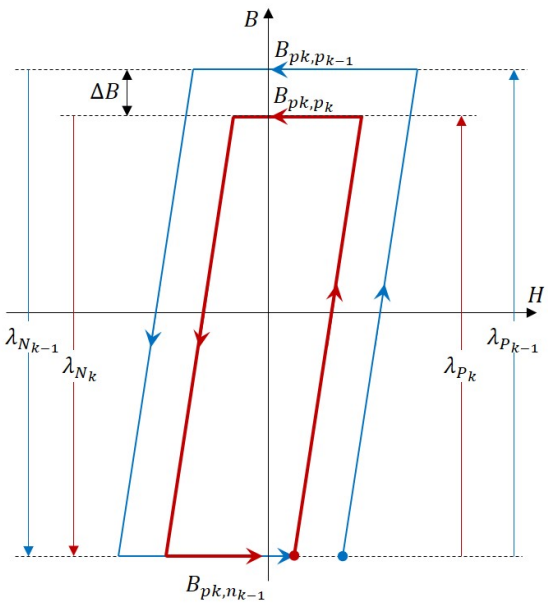

Figure 4: B-H trajectory when a step phase shift change occurs.

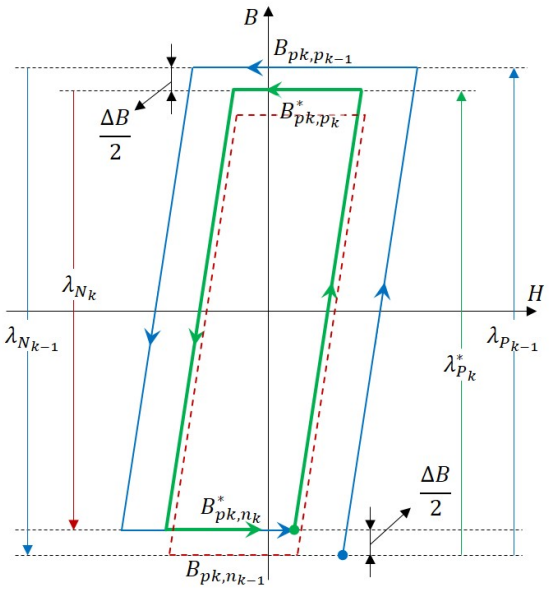

Figure 5: B-H trajectory when the proposed method is applied.

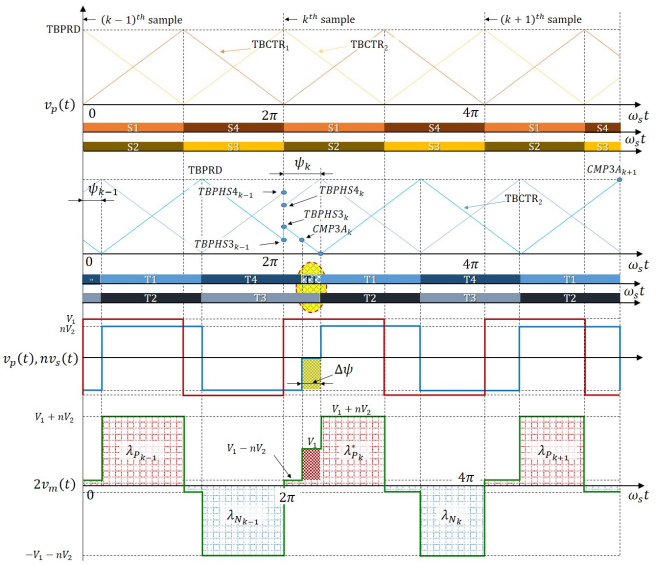

Figure 6: Waveforms by the proposed modulation method when the phase shift increases.

$$B_{pk,p_k} = -B_{pk,n_k} = \frac{\lambda^*_{P_k}}{2N_1A_c} = \frac{1}{N_1A_c\omega_s(1+\sigma)}\left[(\sigma V_1 + nV_2)\pi - 2nV_2\psi_{k-1} - nV_2\Delta\psi\right] \quad (11)$$

Fig. 5 demonstrates the effect of above volt-second product adjustment. As shown, the bias disappears and the flux unbalance no longer exists.

4.2. Implementation

In order to implement the proposed adjustment on the volt-second products, the setting of ePWM modules is slightly changed. Two cases are considered individually: $\Delta\psi > 0$ and $\Delta\psi < 0$.

4.2.1. Phase shift increases

Geometrically, the second part of (10a) and (10b) can be seen as the area of a rectangle with the length of $\frac{\Delta\psi}{\omega_s}$ and the height of $\frac{nV_2}{1+\sigma}$. This area can be removed from $\lambda_{P_{k-1}}$ as (10a) by making the secondary winding voltage $v_s(t)$ zero in exactly $\frac{\Delta\psi}{\omega_s}$ seconds. There are several methods to clamp $v_s(t)$ to zero, the easiest way is forcing an overlapping in the modulation of two legs of Inverter 2 as demonstrated in Figure 6.

As shown in Figure 6, at the beginning of the k^{th} switching cycle, TBPHS3 is updated with the new phase shift value of $TBPHS3_k$ corresponding to the new phase shift ψ_k as normal. Afterward, TBPHS3 starts counting down. When TBPHS3 reaches $TBPHS3_{k-1}$, T_1 should be turned on while T_3 should remain its on state. Because T_1 and T_4 are complementary, as T_1 switches on, T_1 does off. Thus, the gate signals of the transistors T_1 and T_3 become overlapping that clamp output voltage of Inverter 2 to zero. When TBPHS3 reaches zero and TBPHS4 is at peak (equals to TBPRD), T_1 should remain its on state whereas T_3 should be turned off to set T_2 on. This ends the zero volt sub-period of $v_s(t)$ and starts the positive output voltage interval of Inverter 2. The width of this period is

$$\frac{TBPHS3_k - TBPHS3_{k-1}}{TBPRD3} \times \pi$$

which is exactly equal to $\Delta\psi$.

The key of this algorithm is to toggle T_1 (and thus, T_4) at the event TBCTR3 = $TBPHS3_{k-1}$ when counting down. This can be accomplished by using the duty cycle variation mode together with phase shift modulation as follows: assigning the CMPA (counter-compare A) register by $(TBPHS3_k - TBPHS3_{k-1})$ and allowing ePWM3 outputs to toggle at the event TBCTR3 = CMP3A at counting down to turn T_1 on earlier. If there is no actions at TBCTR3 = CAU (counting up), the zero interval appears only in the first half of the k_{th} switching cycle. As a result, the volt-second product of the k_{th} period is modified as desired. If the phase shift remains unchanged in the next sampling period (i.e. $(k+1)^{th}$), the normal SPS modulation should be undertaken. Therefore, CMP3A is assigned as (TBPRD + 1) to disable the toggle action at the event TBCTR3 = CMP3A.

The output is still cleared when TBCTR3 = PRD, thus, it is no need to do any actions when TBCTR3 = ZRO. Table 2 summaries the new configuration of ePWM3 module. Setting of other ePWM modules remain unchanged.

4.2.2. Phase shift decreases

When the phase shift decreases, $\Delta\psi$ is negative. If the above algorithm is applied, a negative value is assigned to CMP3A register. This causes no effect on creating the overlapping interval of the gate signals. Hence, the algorithm needs to be revised for this case.

The switching strategy for this case is illustrated in Figure 7. After a normal synchronized update at the beginning of the k^{th} cycle, TBPHS3 counts down to reach zero. Normally, T_4 is toggled at that event, however here, T_4 should remain on. Thus, the set action at TBCTR3 = ZRO should be disable to avoid a turn-on at this event. At the same time, in the other leg, T_3

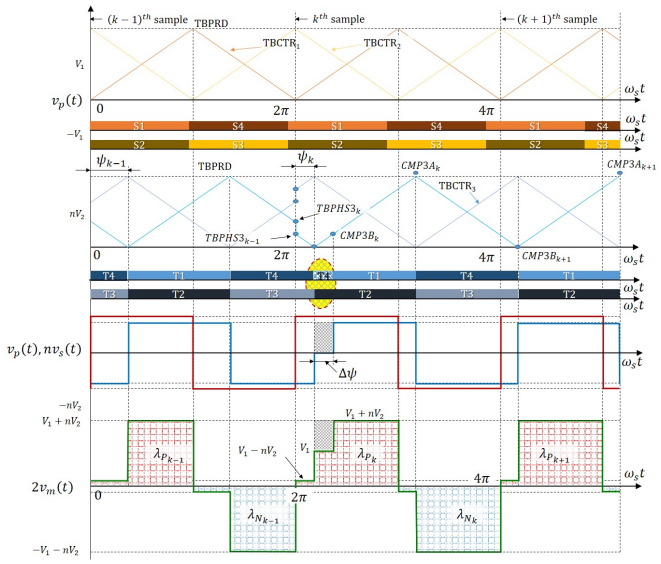

Figure 7: Waveforms by the proposed modulation method when the phase shift decreases.

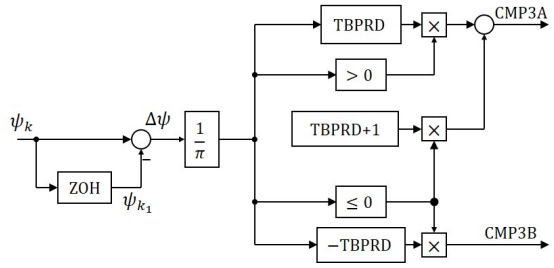

Figure 8: Implementation of the proposed scheme.

goes off and T_2 turns on. The overlapping of T_4 and T_2 helps to clamp $v_s(t)$ to zero. When TBPHS3 equals to $(TBPHS3_{k-1} - TBPHS3_k)$ at counting up, T_4 (and thus T_1) is toggled to end the zero volt interval of $v_s(t)$. The width of this period is

$$\frac{TBPHS3_{k-1} - TBPHS3_k}{TBPRD3} \times \pi$$

which is exactly equal to $\Delta\psi$ as expected.

5. Experimental Results

In order to toggle T_1 and T_4 when TBCTR3 = $(TBPHS3_{k-1} - TBPHS3_k)$ at counting up as mentioned above, duty cycle variation is also used together with the conventional SPS. Since

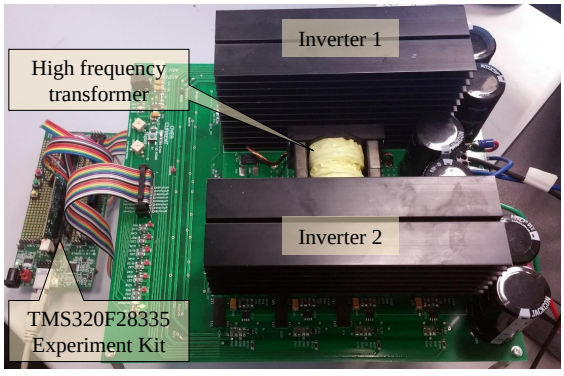

Figure 9: Laboratory-scaled experiment system.

Table 2: Configuration of Action-Qualifier Output 3 registers when $\Delta\psi > 0$.

Event	Old	New	Notes
TBCTR3 = ZERO	Set	Set	N/A
TBCTR3 = TBPRD	Clear	Clear	N/A
TBCTR3 = CAU	Do Nothing	Do Nothing	N/A
TBCTR3 = CAD	Do Nothing	TOGGLE	(i)
TBCTR3 = CBU	Do Nothing	Do Nothing	N/A
TBCTR3 = CBD	Do Nothing	Do Nothing	N/A

Note: (i): CMPA $= \begin{cases} \frac{\psi_k - \psi_{k-1}}{\pi} \times \text{TBPRD}, & \text{if } \Delta\psi > 0 \\ \text{TBPRD} + 1, & \text{if } \Delta\psi \leq 0 \end{cases}$

Table 3: Configuration of Action-Qualifier Output 3 registers

Event	Old setting	New setting	Notes
TBCTR3 = ZERO	SET	Do nothing	N/A
TBCTR3 = TBPRD	CLEAR	CLEAR	N/A
TBCTR3 = CAU	Do nothing	Do nothing	N/A
TBCTR3 = CAD	Do nothing	TOGGLE	(i)
TBCTR3 = CBU	Do nothing	SET	(ii)
TBCTR3 = CBD	Do nothing	Do nothing	N/A

(ii): CMPB $= \begin{cases} \frac{\psi_{k-1} - \psi_k}{\pi} \times \text{TBPRD}, & \text{if } \Delta\psi < 0 \\ 0, & \text{if } \Delta\psi \geq 0 \end{cases}$

the register CMPA has been used for the previous case, CMPB (counter-compare B) register is employed instead. Accordingly, CMP3B is assigned as $(TBPHS3_{k-1} - TBPHS3_k)$, and ePWM3 output is set when TBCTR3 = CMP3B at counting up. Notes that, ePWM3 has already been set to toggle at TBCTR3 = CMP3A at counting down, if CMP3A is smaller than CMP3B, this may cause spurious operation of ePWM3. Hence, CMPA3A is assigned to be TBPRD+1 to disable the toggle action at TBCTR3 = CMP3A. In the consecutive sampling instant, if the phase shift is not changing, T_1 and T_4 should be toggled at TBCTR=ZRO as normal. However, since that action has been disable, CMP3B is thus assigned as zero to re-enable the action in an alternative way. Finally, combined with the previous setting, Table 3 summaries the old and new configurations of ePWM3 module. Those setting must be undertaken at system initialization of the DSP.

The implementation is very simple as depicted in Fig. 8. The deviation of phase shift $\Delta\psi$ is calculated and compared to zero for its polarity. Then, from that, the new value of registers CMP3A and CMP3B are calculated and assigned. Notes that, when there is no phase shift deviation in two consecutive switching periods, $\Delta\psi = 0$, CMP3A = TBPRD+1 and CMP3B = 0 and the normal SPS modulation is conducted.

It can be seen from Fig. 8 and Table 3 that, neither voltage nor current feedback are required. The phase shift deviation is the only necessary information for the above technique. Its deployment is as simple as an additional post-processing procedure of the phase shift before passing to the modulation modules. No new variables or complicated computation are

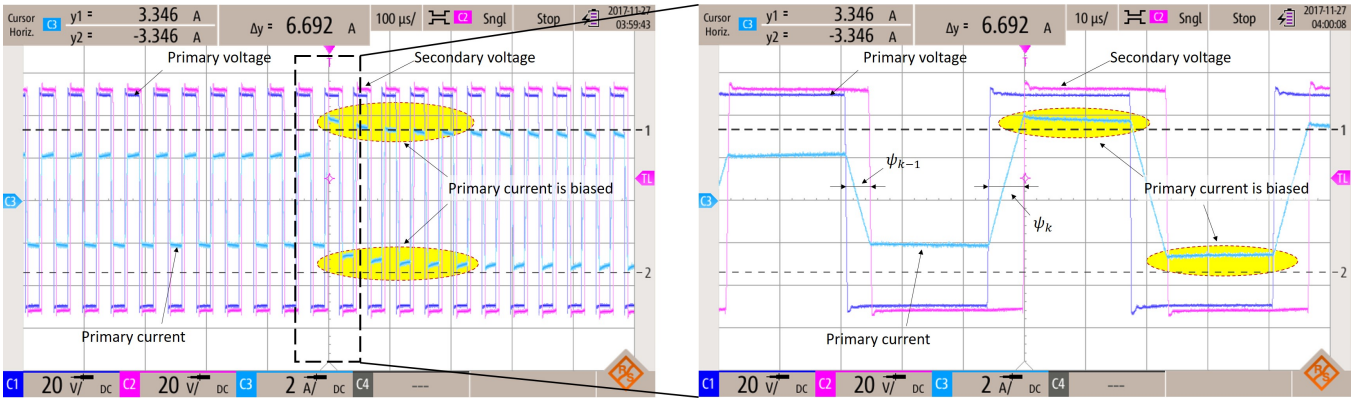

Figure 10: ψ increases, original SPS modulation.

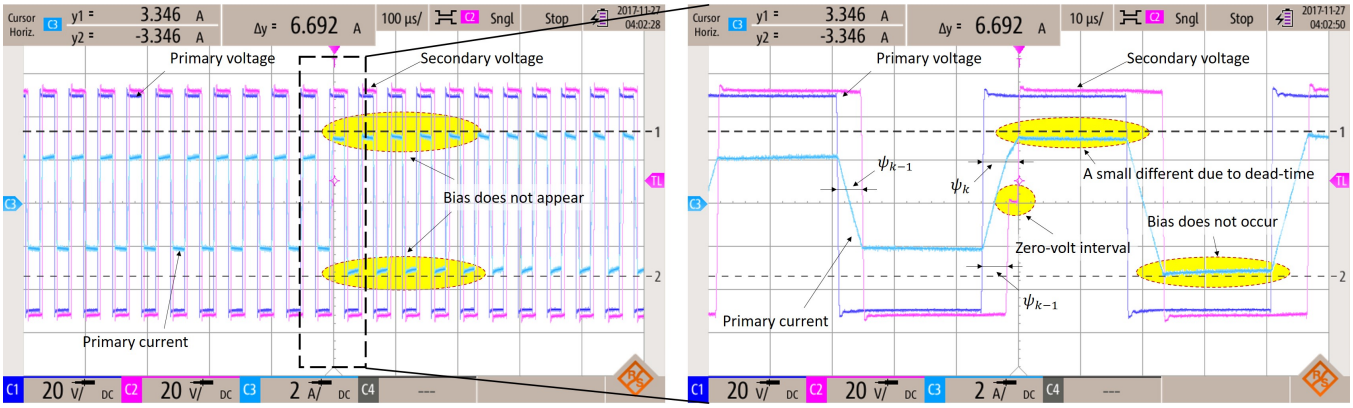

Figure 11: ψ increases, proposed modulation method.

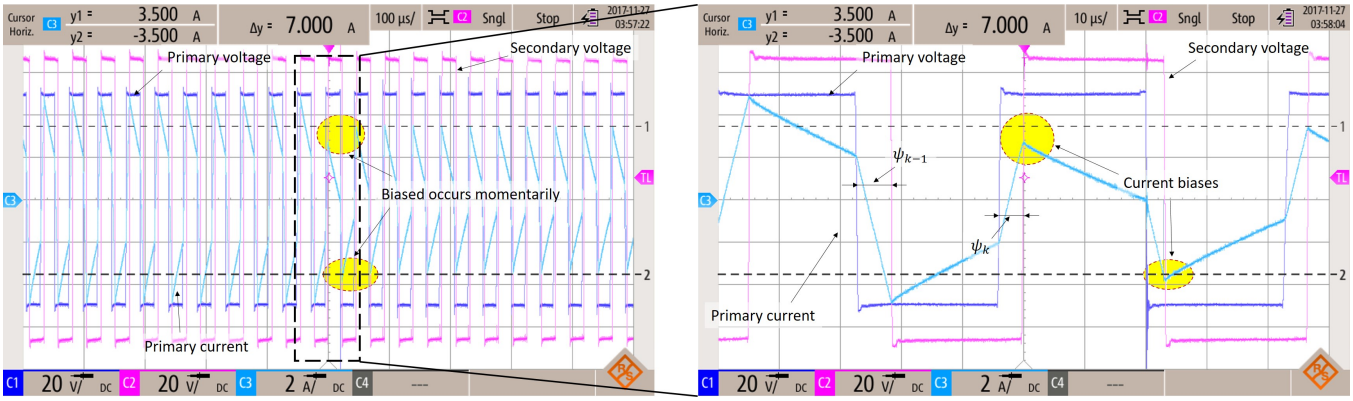

Figure 12: ψ decreases, original SPS modulation.

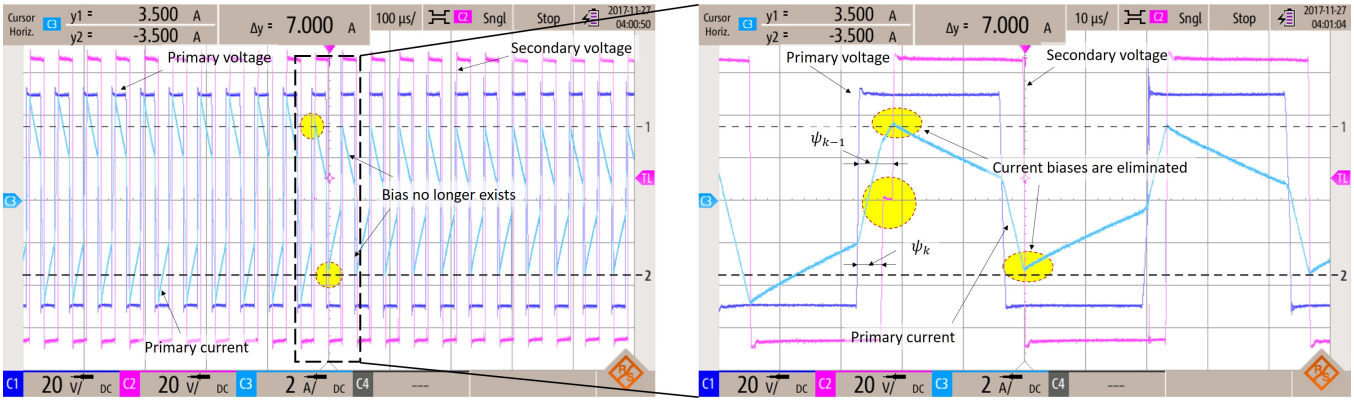

Figure 13: ψ decreases, proposed modulation method.

required. Although four ePWM modules are modulated, only ePWM3 is modified in the run-time for the proposed anti-bias strategy, whereas the setting listed in Table 3 is made at system initialization.

Fig. 9 shows the experiment system used in this study. The switching frequency is 20 kHz and the dead-time is 1 µs. A

programmable power supply is connected to the DC side of Inverter 1. The input voltage is fixed at 50 V. A 30 Ω resistive load absorbs the transferred power at the DC side of Inverter 2. The transformer has two windings wounded on an ETD54/28/19 ferrite core. Shell-typed winding method is used to achieve a high leakage inductance of 90 μH. Since no external inductors is needed, the value of σ is 1. The magnetizing inductance is 1.5 mH and the total AC resistance referred to the primary side, measured at 20 kHz is 50 mΩ. Table 4 lists some main parameters of the system.

A TMS320F28335 experiment kit from Texas Instrument is used to control the system. The setting of the modules ePWM1, 2 and 4 are described in Section 2. Configuration of ePWM3 is as listed in Table 3. Sampling rate is the same as the switching frequency (i.e. 20 kHz). As mentioned above, any changing request in the phase shift from the controller have no effects until the end of the modulation period. Therefore, a sampling rate higher than the switching frequency has no meaning in this circumstance.

5.1. Phase shift increases

Two experiments are conducted: phase shift increases and phase shift deceases. As for the first experiment, the phase shift is initially set at 30 degrees. Consequently, output voltage is about 51.5 V, and transferred power is about 90 W. After some time, the phase shift is suddenly stepped up to 45 degrees. After the transient period, the output voltage is 66.6 V and output power is 150 W. A four-channel, isolated RTH1004 oscilloscope from Rohde & Schwarz is utilized to measure the primary and secondary voltages and currents to examine the bias creation with and without the proposed modulation technique. Figure 10 shows the waveforms obtained with the normal SPS modulation.

As shown in Figure 10, the primary current is well balance before the phase shift increment instant. Since the voltage conversion ratio is almost 1:1, the current has the trapezoidal shape. At the k^{th} switching cycle, the phase shift increases from ψ_{k-1} to ψ_k, the output voltage, however, cannot rise that rapidly as the current shape still has the trapezoidal form. In contrary, the current amplitude changes immediately. The positive peak increases from about 2 A to 4 A, whereas the negative-peak decreases from about -2 A to -2.7 A. Obviously, the current is biased. After about 4 switching cycles (i.e. 200 μs), the bias vanishes and both peaks settle down at ±3.35 A. If the current amplitude is big, that amount of time might be enough to damage the switching devices.

Figure 11 depicts the waveforms obtained when the proposed modulation is applied. At the k^{th} switching cycle, a zero-volt interval in the secondary voltage appears against the step change of the phase shift. The width of the interval is exactly equal to the phase shift deviation. The voltage waveform is thus well matched with the theoretical ones shown in Figure 6. The positive peak current rises from 1 A to 3 A, and the consecutive negative peak is -3.35 A, whereas the peaks of the $(k+1)^{th}$ period and further settle at ±3.35 A as expected. Hence, it can be confirmed that the bias is eliminated within a half of a switching cycle. Notes here that, the positive peak reaches only 3 A instead of the desired value of 3.35 A. This is due to the effect of the dead-time, which is not considered in the above analysis. Discussion on the influence of dead-time on modulation is beyond the scope of this paper.

5.2. Phase shift decreases

As mentioned above, after the transient time, the output voltage is stable at 66.6 V and output power is 150 W with the phase shift of 45 degrees. Now, the phase shift is stepped down back to 30 degrees. Firstly, the proposed method is temporarily disabled to examine the appearance of current bias. Figure 12 describes the waveforms in this case.

Although the phase shift deviation is the same as the previous experiment, the bias appear in this test is smaller and vanishes much faster. By the end of the $(k-1)^{th}$ switching period, the current is still well balance with the current peaks of ±4.9 A. When the phase shift change at the beginning of period k^{th}, the first positive peak reduces to 2.75 A, whereas the negative peak rises to -3.89 A. The current becomes stable in the consecutive period meaning that the bias disappears just after one switching cycle. Although the bias vanish quickly, it causes a momentary hard-transition at the end of the first half of k^{th} cycle because the turn-off current is mostly negative.

When the proposed modulation method is enabled, the bias no longer exists. The positive and negative peaks of the primary current in the k^{th} cycle are 3.65 A and 3.3 A respectively, whereas the expected value is 3.5 A. A zero-volt interval with the width of 15 degrees (equal to the phase shift deviation) appears in the secondary voltage to help balance the current. The experimental voltage waveform once again matches very well with the theoretical plot in Figure 7 which in turns confirms the correctness of the proposed method. Since the bias is eliminated, the momentary hard-transition occurring at the end of the first half of k^{th} cycle is avoided as the turn-off current is greater than zero.

6. Conclusions

This paper discussed about DC bias removal problem for Dual-Active-Bridge DC/DC converters. A new technique was proposed that makes some minor modifications in the setting of only one ePWM module among four of the TMS320F28335 DSP in which the modulation is undertaken. The synchronization update problem of ePWM modules was also addressed. The proposed scheme is very simple as it can be implemented as a small post processing procedure of the control signal before passing to the modulation. No voltage or current information is necessary for the proposed technique. It needs only the deviation of the phase shift which can be obtained easily. Besides, since there is no new additional control variables, the design of the control system is not affected.

Theoretical analysis and experimental results show that, the DC bias is completely remove within just a half of one switching cycle regardless of a increment or decrement of the phase shift. Although the proposed method is applied to modify the modulation pattern of the SPS method on a TMS320F28335 DSP, the same approach can be utilized for other modulation methods, such as DSP or TPS, etc., implemented on different DSPs.

Nevertheless, the proposed technique works as an open-loop method. If the bias is caused by a reason other than pulsating load change, such as unbalanced propagation time of driver, unequal rising/falling time of MOSFETs, different MOSFET parameters, etc., further measurement and processing might be

required as discussed in other publications.

A. Parameters

Table 4: System parameters

Parameter	Symbol	Value	Unit
Trans. ratio	n	1:1	
Inductance	L_s	90	μH
Resistance	R_s	50	mΩ
Nom. frequency	F_s	20	kHz
Nom. phase shift	Ψ	30	deg
Sampling time	T_z	50	μs
Dead-time	T_d	1	μs
DC capacitors	C_1, C_2	1000	μF

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