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Design and Optimization of T-type Converters Using Genetic Algorithm

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Abstract

High efficiency and high power density are becoming increasingly popular in the design requirements of power electronic converters. In this paper, the design and optimization method of a three-phase T-type converter are discussed. Loss models of the converter are formulated by the conventional method. The switching frequency, peak flux density, number of turns, number of layers,..., are optimized using genetic algorithm for minimizing the overall converter loss. Simulation results prove that the loss models are reliable. The optimized converter has improved performance with a high efficiency of up to 99.47% and a low-temperature rise of fewer than 50 degrees Celsius on both inductors and semiconductor devices. The utilization of computer-aided design methods also significantly contributes to reducing the workload of designers.

Keywords: *T-typed converter, optimization, loss models, genetic algorithm.*

1. Introduction

The adoption of electric vehicles (EVs) is seen as a significant means of reducing carbon dioxide (CO2) emissions as they are powered by chemical batteries or supercapacitors instead of fossil fuels [3]. To further enhance the efficiency of EVs, they can be utilized as energy stabilizers, which requires them to be connected to the utility via EV supply equipment (EVSE) that allows for bidirectional transfer of power according to protocols such as CCS. In this research, the focus is on a system in which an EV is connected to the grid using a 12 kW EVSE that is designed to achieve high power density, high efficiency, and bidirectional transfer capability. EVSEs typically consist of both AC/DC and DC/DC converters that are interconnected. A three-phase T-type converter topology was chosen for the front-end stage of the EVSE due to its advantages over other topologies, such as lower losses, better performance, and lower electromagnetic interference [10].

The T-type converter was introduced in 2010 by Schweizer as a potential solution for high-power applications [10]. This topology offers several advantages over traditional diode-clamped three-level topologies, including a reduced number of current-carrying devices due to the elimination of diodes [16]. Compared to the three-level neutral point clamp converter (NPC), the T-type employs an active bidirectional switch to the dc-link voltage midpoint and gets along with two diodes less per bridge leg [9]. As such, it is an alternative to more complex three-level topologies such as active NPCs [1], [6] or split-inductor converters [14]. The T-type converter combines the advantages of two-level converters, such as low conduction losses, small part count, and simple operation principles, with the advantages of three-level converters, such as low switching losses and superior output voltage quality [9].

Although numerous studies on three-phase T-type converters have been published, they have mainly focused on modulation and control strategies. There is a lack of literature that provides a detailed analysis and optimization of the T-type topology. For instance, while [9] reported a low-voltage application of the T-type inverter with a power of 10 kW, the loss breakdown and efficiency were only measured and obtained based on experimental results, not carefully calculated. Similarly, [4], [15], [12], and [11] studied the efficiency of the T-type inverter, but only semiconductor losses were analyzed, and the power dissipated in passive components, such as capacitors and inductors, was not considered. Furthermore, the design usually involves extensive use of experience, and rules-of-thumb and it may require a lot of iterative design time to find the optimum alternative.

The present study provides an in-depth analysis and optimization of the T-type converter, which is commonly used in electric vehicle supply equipment (EVSE). The optimization process focuses on both operation parameters and magnetic devices, with the aim of enhancing the efficiency and performance of the converter. To accurately model the losses caused by semiconductor devices, loss models are formulated using the

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conventional method. The inductors are designed using multi stacks of magnetic cores to increase their volume, which in turn reduces flux density and temperature rise. To improve the accuracy of the copper loss modeling of the inductors, the skin and proximity effects are taken into consideration.

To facilitate this process, power converter design has evolved from a very labor-intensive task to one that relies heavily on computers which reduce the designer's workload. Hence, genetic algorithm is employed, subject to certain inequality constraints. These constraints include the limited window area of the inductor, the specific switching capability of the semiconductor devices, and the operating temperature. The optimized inductor is verified through a finite element method magnetic (FEMM) analysis. The simulation results by LTspice show that the loss models of the semiconductors are reliable. The simulation results obtained through PSIM provide empirical evidence supporting the effectiveness of the designed system at the designed operating point.

2. Steady State Analysis

Fig.1 describes the circuit diagram of a three-phase T-type converter. The main concept of this topology is that zero voltage can be achieved by clamping the output to the ground with a neutral point of the DC bus using 2 bidirectional switches. The inductance value (L) plays an important role in reducing the input current ripple ($\Delta I(\theta)$). In steady state, $\Delta I(\theta)$ is a function of L and switching frequency (f_s), as described in (1):

$$\Delta I(\theta) = \frac{\left(1 - \frac{2V_{ac}(\theta)}{V_{dc}}\right) \cdot V_{ac}(\theta)}{L f_s} \tag{1}$$

where $V_{ac}(\theta) = V_{ac,m}\sin(\theta)$ is the instantaneous grid voltage, V_{dc} is DC bus voltage, $\theta = (\omega t + \phi)$ is a phase of grid voltage. The maximum ripple current (ΔI_m) can be calculated by solving the derivative of (1) equal to zero, as described in Equation (2):

$$\Delta I_m = \frac{V_{dc}}{8 f_s L} \tag{2}$$

The inductance value thus can be selected from allowable current ripple, following (3):

$$L = \frac{V_{dc}}{8 f_s \Delta I_m} \tag{3}$$

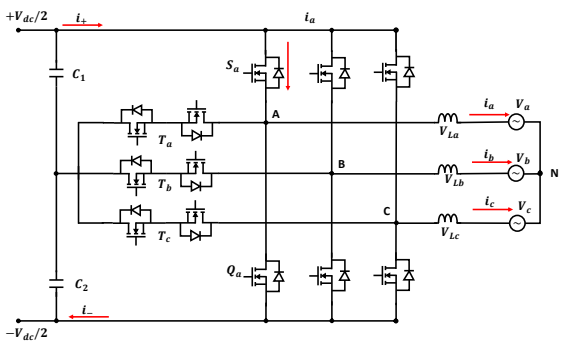


Figure 1. Three-phase T-type converter topology

The average current ripple (ΔI_{avg}) is obtained when integrating (1) over the whole period, as described in (4):

$$\Delta I_{avg}(\theta) = \frac{V_{ac}}{f_s \cdot L} \cdot \left(\sin\theta - \frac{2V_{ac}}{V_{dc}} \cdot \sin\theta^2\right) \tag{4}$$

The maximum flux swing is described in (5):

$$\Delta B = \frac{V_{ac}}{f N A_c}\left(1 - \frac{2V_{ac}}{V_{dc}}\sin\theta\right)\sin\theta \tag{5}$$

where N is the number of turns of the winding; A_c is the cross-section area of a magnetic core, assuming that the toroidal core is used.

The average currents through each switch, average grid current, and root-mean-square current of the switches and capacitor are calculated by equations from (2) to (5), applying the method reported in [8], which using effective duty cycle (d_{rms}) independent of the switching action.

To enable derivation of the proposed model, the following assumptions are required:

1. the T-type converter is assumed to operate in continuous conduction mode,
2. the line current is assumed to be in phase with the input line voltage – i.e. a sinusoidal waveform is assumed with only linear switching ripple,
3. an efficiency of 100% is assumed.

d_{rms} is a function of the half-line frequency phase angle given by (6):

$$d_{rms} = \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi}\left(1 - \frac{2V_{ac}(\theta)}{V_{dc}}\right)^2 dt} \tag{6}$$

The root-mean-square current of switches can be calculated by the following equations and (7) and (8):

$$I_{D,rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(I_{pk}\sin\theta \cdot \frac{2V_{ac}}{V_{dc}}\sin\theta\right)^2 dt} \tag{7}$$

$$I_{T,rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(I_{pk}\sin\theta \cdot d_{rms}\right)^2} \tag{8}$$

where $I_{pk} = I_g \cdot \sqrt{2} + \frac{\Delta I_m}{2}$

The root-mean-square of capacitor current is given by (9):

$$I_{C,rms} = I_{L,rms} \cdot \sqrt{\frac{V_{ac}(\theta)}{2V_{dc}} \cdot \left(\frac{1}{\pi} + \left(\frac{4}{\pi} - \frac{3V_{ac}}{4V_{dc}}\pi\right)\right) dt} \tag{9}$$

where $I_{L,rms}$ is the inductor rms current, can be calculated as (10):

$$I_{L,rms} = \sqrt{I_g^2 + \frac{\Delta I_{avg}^2}{12}} \tag{10}$$

3. Inductor Design

At the first step, some preliminary parameters must be determined:

- initial inductance value,

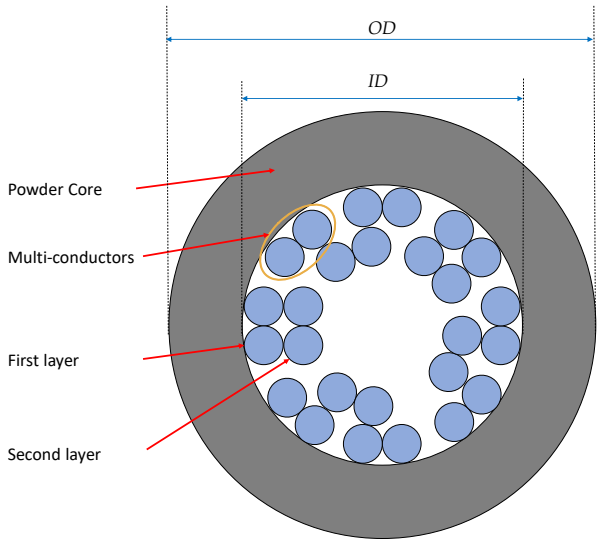


Figure 2. Toroidal core with multiple strands and multiple layers

- current density ($J = 4 - 10$ A/m),
- window utilization factor ($k_u = 0.2 - 0.6$ for inductor),
- initial switching frequency and flux density.

After that, from (3), (10) and (16), the core size and winding wire size can be selected according to Ap or Kg methods [7]. To reduce the AC resistance (R_{AC}), multiple strands of wires are used as shown in Fig.2. Besides, to reduce peak flux density and temperature rise (T_r), multiple stacks of the core are designed.
According to [7] the number of turns can be calculated by (11):

$$N = ceil\left(\frac{V_{dc}}{8 f_s \Delta I_m} \cdot \frac{\mu \mu_0 A_c}{MPL}\right) \tag{11}$$

where $\mu_0 = 4\pi 10^-7$ is magnetic permiability; μ is relative permiability; MPL is magnetic-path-length of the magnetic core; and A_c is cross-section-area of the magnetic core.
The possible number of turns that can be obtained from each layer is described in (12):

$$N_n = \frac{\pi\,[ID - 2(n-1)d_w]}{d_w n_{str}} \tag{12}$$

where N_n is possible number of turns of n^{th} layer; ID is inner diameter of toroidal core; d_w is wire diameter; n_{str} is number of wire.
Let m is number of layers of winding, m can be determined by (13):

$$m = n_{min} \tag{13}$$

with the following condition, as described in (14):

$$N - \Sigma N_{n_{min}} < 0 \tag{14}$$

where n_{min} is minimum value of n that (14) is satisfied.
The window area factor (k_u) should be limited as showed in (15):

$$N d_w n_{str} < W_a k_{u,m} \tag{15}$$

The inductor must be designed to avoid working at saturation area, so the maximum flux density (B_m) is limited by (16):

$$B_m = \frac{V_{ac}}{2 f N A_c}\left(1 - \frac{2V_{ac}}{V_{dc}}\sin\theta\right)\sin\theta < B_{sat} \tag{16}$$

4. Power Loss Modeling

4.1. Power Electronics loss

The overall power dissipation on the Silicon-Carbide Metal–Oxide–Semiconductor Field-Effect Transistor (SiC-MOSFETs) can be estimated by (17):

$$\Delta P_{mos} = \Delta P_{cond} + \Delta P_{sw} + \Delta P_{rev} \tag{17}$$

where ΔP_{cond}, ΔP_{sw} and ΔP_{rev} are conduction loss, switching loss, and reverse recovery loss respectively, as shown in (18), (19), and (20):

$$\Delta P_{cond} = 6 \cdot R_{ds,on}(I_T^2 + I_Q^2) \tag{18}$$

$$\Delta P_{sw} = 3 \cdot \frac{1}{2}\frac{V_{dc}}{2}\frac{I_{s,avg}}{2}(t_r + t_f) f_s \tag{19}$$

$$\Delta P_{rev} = 3 \cdot \frac{1}{4}\frac{V_{dc}}{2} Q_{rr} f_s \tag{20}$$

where $R_{ds,on}$ is ON resistance of the MOSFET; t_r and t_f are rising and falling time of the MOSFET respectively; Q_{rr} is reverse recovery charge of the MOSFET. All are given in the semiconductor datasheet.

4.2. Inductor Loss

Inductor loss includes ferrite loss on the magnetic core and copper loss dissipating on windings as (21):

$$\Delta P_L = \Delta P_{fe} + \Delta P_{cu} \tag{21}$$

where ΔP_{cu} and ΔP_{fe} are the winding loss (or copper loss) and core loss (ferrite loss). From [2], the core loss can be estimated by (22):

$$\Delta P_{fe} = 3 \cdot B_{avg}^a (b f_s + c f_s^d) \cdot g \tag{22}$$

where g is the weight of the toroidal core; a,b,c, and d are the core loss coefficients. The copper loss is calculated by (23):

$$\Delta P_{cu} = 3 \cdot (R_{dc} I_{L,rms}^2 + R_{ac}\frac{\Delta I_{avg}^2}{12}) \tag{23}$$

The DC resistance is given by (24):

$$R_{dc} = (MLT) N \frac{r_{str}}{n_{str}} \tag{24}$$

where r_{str} is the resistance density of a strand; and MLT is the mean-length-turn of the magnetic core.
The AC resistance depends strongly on the switching frequency and the winding geometry by the skin and proximity effects. According to [13], the AC resistance can be estimated as (25):

$$R_{ac} = R_{dc}(A_{str}\sqrt{\frac{\sinh 2A_{str} + \sin 2A_{str}}{\cosh 2A_{str} - \cos 2A_{str}}} + \frac{2}{3}(n_{str} \times m^2 - 1)\frac{\sinh A_{str} - \sin A_{str}}{\cosh A_{str} + \cos 2A_{str}}) \tag{25}$$

where $A_{str} = \frac{1}{\delta}\left(\frac{\pi}{4}\right)^{0.75}\sqrt{\frac{d_b^3}{d_w}}$; δ is skin depth; $\delta = \frac{6.62\times 10^{-2}}{\sqrt{f_s}}$

4.3. Capacitor Loss

Due to the converter's output current ripple, the ripple will be filtered out by DC link capacitors, which will dissipate some power on the series resistance of capacitors. The capacitors loss is calculated using (26):

$$\Delta P_{\text{cap}} = (ESR) \cdot I_{\text{c,rms}}^2 \tag{26}$$

where ESR is the series resistance of the capacitor.
Finally, the total power dissipation of the converter is derived as (27) :

$$\Delta P_{tol} = \Delta P_{mos} + \Delta P_L + \Delta P_{cap} \tag{27}$$

5. Optimization

The overall power dissipation should be minimized to maximize system efficiency. The inductor is designed as described in Section III for a given input parameters $(V_{dc}, V_{ac}, P_{rate})$, the tuning parameters are f_s, V_{dc} and L. Here, some additional constraints are considered as well. First, after designing the inductor, according to [7], the temperature rise of the core can estimated by (28):

$$\Delta T_L = 450 \left(\frac{\Delta P_L}{A_t} \right)^{0.826} \tag{28}$$

where At is the surface area of the inductor.
If the thermal resistance of the heatsink R_{hs} is given, the temperature rise of power semiconductors devices can also be estimated. Assuming that the heat generated from semiconductor devices is evenly distributed on the heatsink, then the temperature rise is shown in (29) :

$$\Delta T_{mos} = R_{hs} \Delta P_{mos} \tag{29}$$

A certain allowable value of ΔT_{max} should not be exceeded by the maximum temperature rise, as shown in (30):

$$\max(\Delta T_L, \Delta T_{mos}) < \Delta T_{max} \tag{30}$$

Due to the limitation on tolerance of the semiconductor, the DC bus voltage V_{dc} should be limited at 900 V. The minimum of V_{dc} is determined based on the average voltage behind the rectifier, then the value 650 V is selected for the minimum DC bus voltage.
To avoid the shoot-through phenomenon in the MOSFET bridge, the switching frequency should be limited by (31):

$$f_s < \frac{1\%}{t_{dead}} \tag{31}$$

Now the optimization problem is defined as follows:

*) Minimization problem:
Find a set of (f_s, V_{dc}, L) to minimize the total converter loss:

$$f(f_s, V_{dc}, L) = \Delta P_{tot} \rightarrow min \tag{32}$$

subject to:

$$\begin{cases} c_1(f_s, V_{dc}, L) = f_s - F_{s,max} \leq 0 \\ c_2(f_s, V_{dc}, L) = V_{dc} - V_{dc,max} \leq 0 \\ c_3(f_s, V_{dc}, L) = V_{dc,min} - V_{dc} \leq 0 \\ c_4(f_s, V_{dc}, L) = \max(\Delta T_L, \Delta T_{mos}) - \Delta T_{max} \leq 0 \\ c_5(f_s, V_{dc}, L) = k_u - k_{u,m} \leq 0 \end{cases} \tag{33}$$

*) Optimization algorithm:
There are many approaches available to solve the optimization challenges mentioned above. However, because it includes a round-up (ceiling) function, it should be noted that the optimizing function is not continuous nor differentiable at this point. Therefore, explicit methods based on a gradient are not applicable; instead, heuristic techniques such as the genetic algorithm (GA), differential evolution (DE), and particle swarm optimization (PSO) are preferred [5]. In this paper, GA is selected due to its simplicity and feasibility. Flow chart diagram of the whole optimization and design process is given in Fig.3.

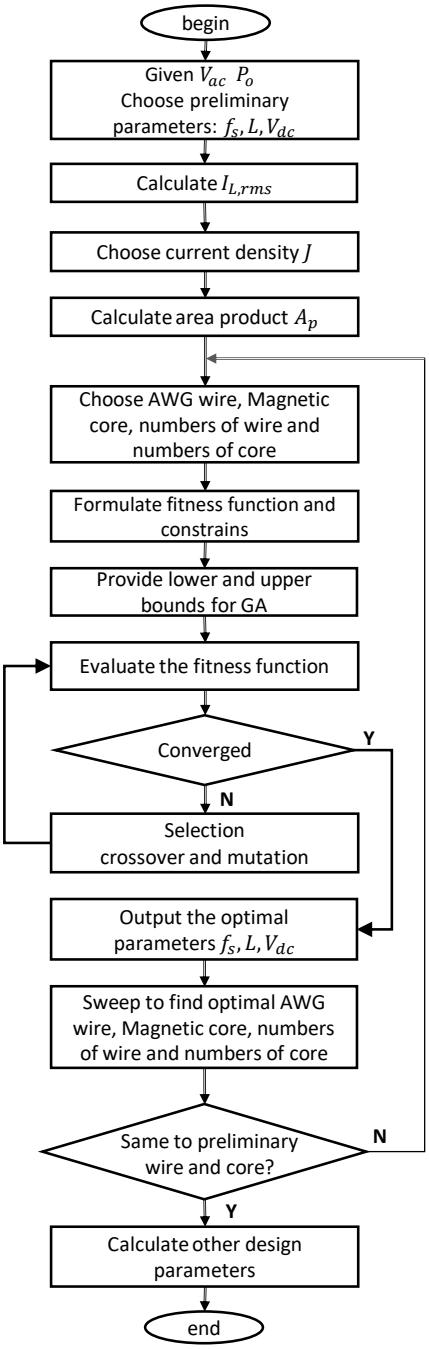


Figure 3. Design and optimization flow chart

Table 1. Specification and preliminary parameters

Parameter	Symbol	Value
Input Voltage	V_{ac}	220 V
Rated Power	P_{rate}	12 kW
Switching frequency	30	kHz
Peak flux density	B_m	0.7 T
Inductance value	L	500 μH
Desired current density	J	550 A/mm^2
Maximum temp. rise	ΔT_{max}	50° C
Selected wire		AWG 14
Selected toroidal core		CS467060
SiC MOSFET		C2M0025120D

Table 2. Lower and upper bounds for genetic algorithm

Parameter	Symbol	Lower Bound	Upper Bound
DC bus voltage	V_{dc}	650 V	900 V
Switching frequency	f_{sw}	10 kHz	3.3 MHz
Max. flux density	B_m	0 T	0.7 T
Number of variables		3	
Population size		100	
Number of generations		30	
Creation function		constraint dependent	
Scaling function		fitness scaling	
Selection function		stochastic uniform	
Mutation function		constraint dependent	
Crossover function		constraint dependent	

Table 3. Optimized and modified parameters

Parameter	Symbol	Opt. Value	Mod. Value	Unit
Switching frequency	f_s	22.1	20	kHz
Inductance value	L	718	718	μH
DC bus voltage	V_{dc}	651.6	650	V
Number of turns	N	36	36	turns
Number of wires	n_{str}	2	2	strands
Mosfet loss	ΔP_{mos}	44.50	44.68	W
Inductor loss	ΔP_L	31.09	31.68	W
Total loss	ΔP_{tot}	76.55	77.81	W
Inductor temp. rise	ΔT_L	33.65	33.77	°C
Heatsink temp. rise	ΔT_L	40.65	40.8	°C
Efficiency at P_{rate}	η	99.36	99.35	%

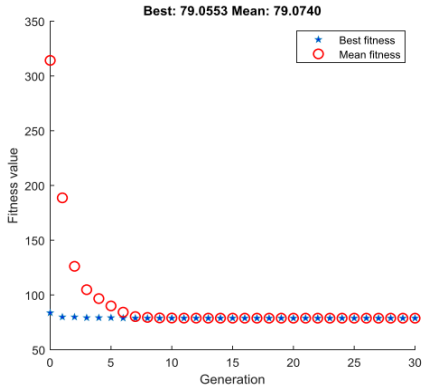


Figure 4. Optimization process using genetic algorithm

6. Result and Discussion

6.1. Optimal Result

A design and optimization technique for battery charging applications was proposed and used to design a 12 kW, three-phase T-type converter. The rms current was calculated using Equation (10) and a current density of 5.5 A/mm^2 was chosen. The magnetic core selected for the design was the CS467060 from Changsung Corporation. Table 1 presents the preliminary parameters and specifications of the converter.

Table 2 presents the lower and upper boundaries for the optimization variables, which were determined through a rigorous algorithm. The optimization algorithm's progress is depicted in Fig. 4. The optimum loss of 79.06 W was achieved at a switching frequency of 22.1 kHz, an inductance of 718 μH, and a DC bus voltage of 651.6 V. The highest efficiency of 99.36% was achieved at the rated power of 12 kW. Furthermore, the temperature rise of the inductor was calculated as 33.77 degrees, which meets the maximum allowable value outlined in Table 2. Additional parameters are outlined in Table 3.

It was rounded down to 20 kHz because 21.1 kHz is unsuitable for programming. Due to this, the converter's efficiency and total loss deviate slightly from their ideal values. That variation, though, is negligible and can be ignored. The modified optimal parameters and all other design parameters are described in Table 3.

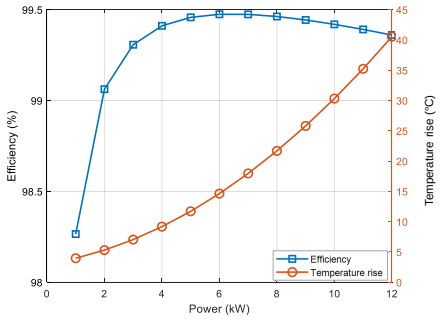
The efficiency and temperature rise curves derived using the optimized and modified parameters are shown in Fig.5. As shown in this Fig.5a, the maximum efficiency of nearly 99.47% was achieved at around 6 kW. The expected efficiency at the rated power was 99.36%, as mentioned above. The plotted temperature curve indicates the trend of the greater value between the temperature of transformers and power electronics devices. At the rated power, the temperature rise was about 40 degree Celsius. With the assumption that the ambient temperature is 25 degree Celsius, the hottest spot was about 85 degree Celsius. The characteristics are the same when considering the modified parameter set. However, the efficiency is expected to be slightly lower while the temperature rise is a little bit less than that when applying the optimized parameter set., as can be seen in Fig.5b.

The integration of computer support enables the automation of the optimization process, leading to a substantial reduction in the designer's workload during the design process.

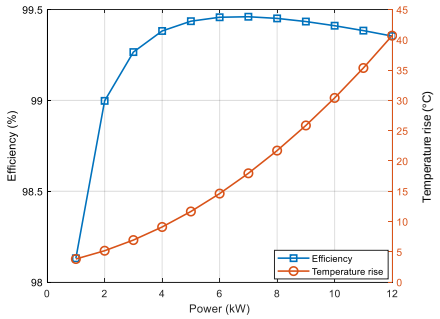
6.2. Simulation Results

A Finite-Element Analysis (FEA) was carried out to verify the designed inductors using the Finite-Element-Method-Magnetic (FEMM) version 4.2. The simulation results are presented in Fig.6, which shows the flux density distribution in the inductor. The peak flux density was found to be 591 mT, which meets the saturation condition. However, this value is 11% higher than the calculated value of 525 mT. This discrepancy is attributed to the uneven distribution of flux density, where the inner edge of the core has a higher flux density, while the outer edge has a lower density. The calculated value represents the average flux density and is therefore lower than the maximum density obtained in the simulation.

The FEA results also demonstrate that other parameters such as inductance, AC resistance, copper, and ferrite losses closely match the designed values. A comparison between the calculated and simulated results is presented in Table 4, which indicates a high level of agreement between the FEA simula-



(a)



(b)

Figure 5. Calculated efficiency and temperature obtained by: (a) optimized parameters (b) modified parameters.

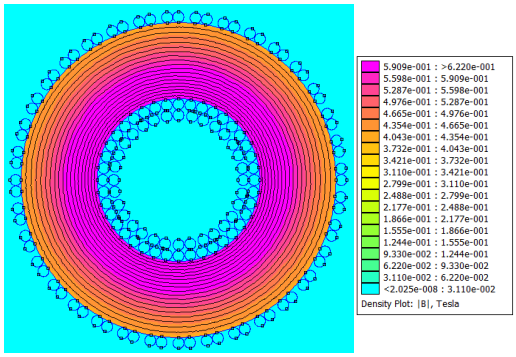
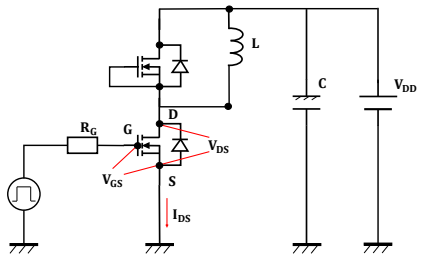


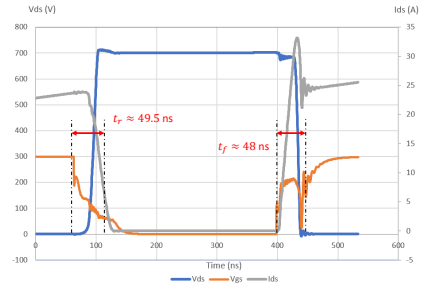
Figure 6. Finite-element-analysis using FEMM 4.2.

tion and the theoretical calculations. The simulated inductance was 722 μH, which is only 0.6% higher than the expected value of 718 μH. Furthermore, the predicted inductor losses were also in close agreement with the FEA simulation results. Thus, it can be concluded that the converter models and optimization strategy presented in the previous sections are valid and reliable.

The loss models of semiconductor devices were validated through simulation using LTspice software, version XVII. A double-pulse-test (DPT) circuit was implemented as depicted in Fig.7a where the DPT inductor L was set to the value of one in a T-type converter. The device under test (DUT) was Q_2, a semiconductor device used in power conversion. To validate switching loss, the inductor current (I_{L_D}) was raised to the average current of the MOSFET in the T-type converter. The drain-source current (I_{ds}) and drain-source voltage (V_{ds}) were monitored and are shown in Fig.7b. A 10 Ω gate resistor was selected to achieve a rise time (t_r) and fall time (t_f) of



(a)



(b)

Figure 7. Simulation of DPT circuit by LTspice: (a) DPT circuit (b) DPT waveforms.

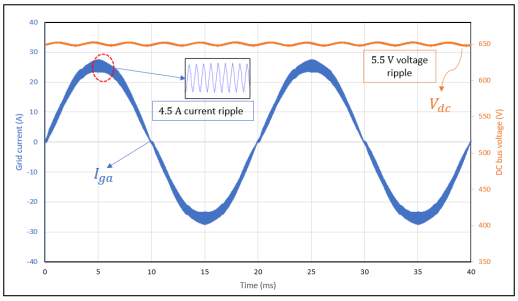


Figure 8. Input current and output voltage waveform

approximately 50 ns, consistent with their selected values in (19). The simulation results confirmed the reliability of the loss models of semiconductors in the T-type converter.

Subsequently, the system's operation was validated through simulation using PSIM version 9.11. The simulation was carried out with an AC input voltage of 220 V and a frequency of 50 Hz while maintaining the output power at 12 kW with an output resistance of 36.5 Ω. As described in Fig.8, the input current was sinusoidal, with a low current ripple of 4.5 A, attributable to the large inductance value. The total harmonic distortion of the input current was found to be 5%, satisfying harmonic standards such as IEEE 519-2014. the input power factor was near unity at 0.9987. The DC bus voltage was stable at approximately 650 V. These results serve as confirmation that the designed converter can operate efficiently.

Table 4. Design validation

Parameter	Symbol	Calculation	Simulation	Unit
Inductance	L	718	722	μH
AC resistance	R_{ac}	0.224	0.22	Ω
DC resistance	R_{dc}	0.026	0.026	Ω
Ferrite loss	ΔP_{fe}	1.35	1.32	W
Peak flux density	B_m	0.53	0.59	T

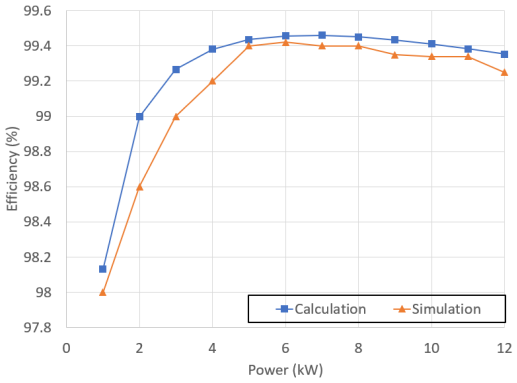


Figure 9. Efficiency comparison between calculation and simulation

The simulation efficiency was compared to the calculations, and good agreement was observed in the mid and high-power ranges. In the low-power range, the simulation efficiency was found to be less than that of the calculated efficiency by less than 0.4%. This small discrepancy can be ignored. Overall, these simulation results validate the converter models and optimization strategy presented in the earlier sections.

Conclusion

In this paper, a comprehensive loss model for T-type converters in three-phase power systems was presented. To minimize the converter loss, an optimization strategy was developed, which involved optimizing three key variables, namely the switching frequency, DC bus voltage, and inductance value. Nonlinear inequality constraints were also taken into account during the optimization process. A genetic algorithm was chosen to optimize the converter as the optimizing function was highly nonlinear. To evaluate the reliability of the converter model, finite-element analysis was conducted. The optimized converter demonstrated superior performance, achieving an efficiency of up to 99.47% and a temperature rise of fewer than 50 degrees Celsius for both the inductor and semiconductor devices. Overall, this paper provides valuable insights into loss modeling and optimization strategies for T-type converters in three-phase power systems. The design method based on computer-aided also helps reduces the designer's workload.

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