Vol 5 (1) (2024)

Measurement, Control, and Automation

Website: https:// mca-journal.org

ISSN 1859-0551

Start-up Procedure for the Three-Phase Four-Leg Inverter in an AC Battery application

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Abstract

Three-Phase Four-Leg Inverter is getting so much attention due to its ability to deal with unbalanced AC voltage sources that can be caused by grid/load faults. Recently, the flexibility of this converter to connect both the 1-phase and 3-phase grid systems in a home battery application has further concern. A vast amount of literature that deals with this topology is exclusively focused on various modulation methods and control structures aimed at optimizing different aspects of its steady-state and/or transient performance. However, no literature is available on its start-up procedure in grid-tied mode which is an indispensable part of the control design of any practical circuit. To fill this gap, in this paper, a three-step start-up procedure for a three-phase four-leg Inverter in an AC Battery is proposed. The primary goal is to ensure that the inrush currents stay below a specific level while the output voltage increases to its reference value with a small overshoot. The proposed start-up procedure is illustrated via Hardware-in-the-loop (HIL) simulation results, which improves the feasibility of future experiments.

Keywords: *AC Battery, Hardware-in-the-loop, Three-Phase Four-Leg Inverter, Start-up Procedure*

Symbols

V_{dc_ref}	V	Reference DC Voltage
V_{ref}	V	Reference for modulation module

Abbreviations

PFC	Power Factor Correction
PV	Photovoltaic
AC	Alternating current
DC	Direct current
HIL	Hardware in the loop
DSP	Digital signal processing
OCP	Over current protection

1. Introduction

In recent years, the home battery has gained great interest thanks to its economic viability of capacity sharing [1] and increasing energy self-consumption [2-4]. This residential application is a combination of photovoltaic (PV) systems and an energy storage system using battery. There are two solutions for this application: AC-Coupled and DC-Coupled. This paper focuses on the AC-Coupled one because it can be easily retrofitted with the domestically installed PV system, its flexibility with extended modules, and isolation for the battery system. Furthermore, some companies have introduced a product named AC Battery that integrates both the battery and the power converter inside. A requirement of an AC Battery is the ability to connect to both 1-phase and 3-phase grid cords as well as operate properly in multiple conditions. To achieve that goal, this paper has selected the two-stage topology for the power energy conversion, and the three-phase four-leg (3P4L) structure is chosen for the Power Factor Correction (PFC) stage. This converter can be flexibly transformed into the 1-phase structure with two interleaved H-bridges [5]. In addition, the 3P4L has the capability of handling unbalanced loads in energy storage applications [6]. Literature on this subject mainly focuses on different control structures and modulation algorithms to deal with specific problems [8-11]. The start-up procedure is another important issue for operating the power converters [12]. However, the start-up control methods in the grid-connected mode of the three-phase four-leg inverter have not been a concern in the previous literature. Some research about this topic is only for the Three-Phase Three-Leg Inverter and different topologies of boost PFC converters [13-16]. One reason for this lack of academic community interest in start-up control issues might be the perception

Received: 20 September 2023; Accepted: 09 November 2023.

that the start-up control can be done easily with the traditional reference voltage ramp method. However, this is not entirely true. For some control structure that uses a modulation method with a low modulation index, using the conventional approach can be very challenging since there will not be enough DC voltage in the bulk capacitor after charging by the diode rectifier to perform the modulation.

In this paper, a detailed three-step start-up procedure for the three-phase four-leg inverter in the AC Battery is proposed. In the first step, the DC-link capacitor is charged by the three-phase bridge diode rectifier via precharge resistors, which are used to limit the charging currents. In the next step, the precharge resistors are shorted using in-rush current relays. Finally, the DC-link voltage is controlled by the DSP-controlled system to increase the reference value with a neglectable overshoot. Two different approaches to control the DC-link voltage in this final step, namely the Reference Voltage Ramp (The traditional method) and Constant Duty Cycle Ramp will be discussed. The reference voltage ramp start-up method will be mentioned first to show the props and cons of the traditional approach, while the constant duty ramp method will be introduced later to provide a solution to the problem that arises with the previous one. Matlab/Simulink simulation and Typhoon HIL + DSP experiment are also carried out on two different modulation methods, one with a high modulation index (Conventional Three-Dimensional Space Vector Modulation) and one with a low modulation index (Remote State Pulse Width Modulation) to verify the proposed start-up procedure in different situations.

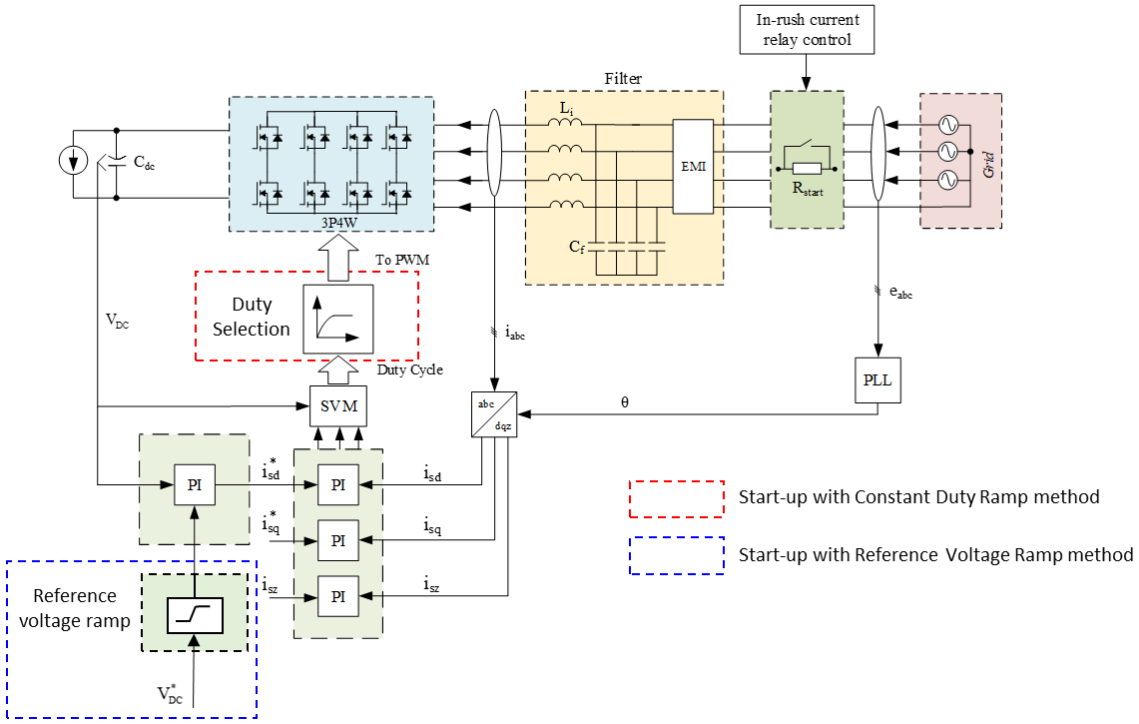

Figure 1: Control structure of the Three-Phase Four-Leg inverter

2. Main research

2.1. Power circuit and control of the system

The power circuit and control structure of a three-phase four-leg inverter is shown in Figure. 1. In this design, a basic Voltage-Oriented Control (VOC) control topology with two control loops is used to achieve PFC performance and ensures the output DC-link voltage increases to its reference value. Two modulation methods, one with high modulation index (Conventional Three-Dimensional Space Vector Modulation [8]) and one with low modulation index (Remote-State Pulse Width Modulation [9]), are discussed to point out the advantages and disadvantages of different start-up methods. A start-up module is added after the SVM module to avoid significant DC voltage overshoot and limit the inrush currents. The control structure is implemented with a digital signal processor (DSP) TMS320F28379D from Texas Instrument (TI) [17]. The phase currents and the grid voltages are sensed and converted to digital signals using the 12-bit Analog-to-Digital Converter (ADC) of the DSP. These digital signals are then used as input for the control program written in the Control Law Accelerator (CLA) of the DSP. The calculated duty cycles from the CLA will be fed into the enhanced Pulse Width Modulation (ePWM) to determine the gate signals for the upper and the lower switches of the Three-phase Four-leg power circuit.

2.2. Start-up procedure

This start-up procedure is presented in Figure 2, the DC-link capacitor charges from 0V to the reference value in three steps. Firstly, when all the switches are turned off, the DC-link capacitor charges slightly below the peak value of the line grid voltage using the bridge diodes of the switches and the start-up resistor. This resistor is used to limit the inrush current through the DC-link capacitor below the Over-Current Protection level and its value can be chosen in the worst case, i.e., when the grid voltage stays at its maximum value.

Secondly, the inrush current relays are turned on to comment the start-up resistors out of the system, hence the output voltage increases to the peak value of the phase-phase grid voltage. A short delay is applied after the relays are turned on to ensure enough time for the current transients to settle. Finally, the DC-link capacitor charges to its reference value by enabling the operation of the control loop. Two approaches to control the switches so that the PFC input currents and the DC output voltage do not experience abrupt changes, namely reference DC voltage ramp (the traditional method) and constant duty ramp (Set Duty) will be discussed respectively in the next subsection.

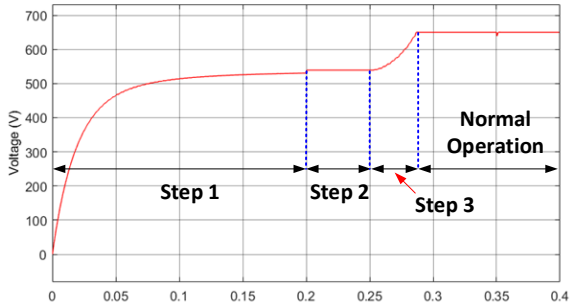

Figure 2: DC Output voltage during the start-up procedure

2.3. *Reference DC voltage (V_{dc_ref}) ramp*

This method has been widely used in most PFC structures that need to charge the DC capacitor to the reference value. The idea of this method is to ramp the output voltage by ramping up its reference value from the last value at the end of the second step to the desired value. Without the ramp process, the DC voltage response may experience a large overshoot as shown in Figure 3 and the inductor currents will exceed the Over-Current Protection (OCP) level due to the step reference. The big difference between the reference value and the present DC voltage value results in a large DC voltage controller output, which makes the control loop overreact to the drastic change and causes a big voltage overshoot and current spikes.

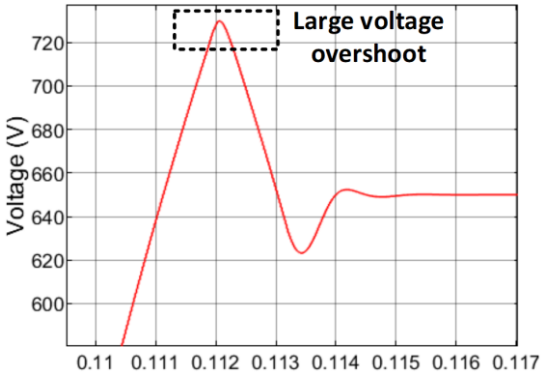

Figure 3: DC voltage response when a step reference is applied.

As can be seen from Figure 4, by adding the ramp block to gradually increase the reference voltage to the desired value, the unwanted overshoot voltage current spikes are almost canceled out. It is very clear that the strength of this approach comes from the simplicity of this method since it requires only a ramp module to achieve the desired start-up performance. Note that these are simulation results for a Three-Phase Four-Leg Inverter using a Three-Dimensional Space Vector Modulation (SVM-3D) modulation strategy.

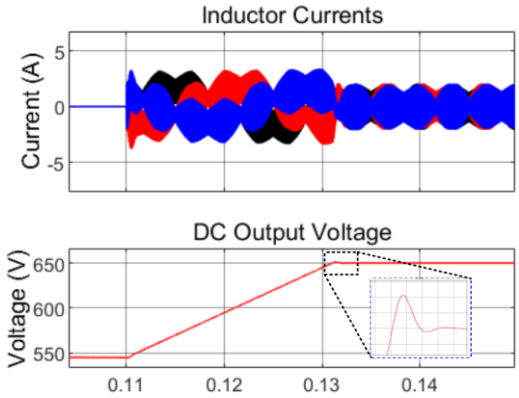

Figure 4: Matlab/Simulink simulation results of DC voltage, and inductor currents when the reference DC voltage ramp process is added

Although this method can reduce the charging current and make the output voltage increase steadily, it utilizes the duty cycles calculated from the SVM module and some modulation methods with low modulation index can raise difficulties for the system to remain in the stable region. For example, a known modulation method that is used to limit the leakage current in the Three-Phase Four-Leg PFC Inverter (RSPWM) [9] has the modulation index m within the range [0;1], with the modulation index defined as in (1):

$$m = \frac{2V_{ref}}{V_{DC}} \quad (1)$$

Where: V_{ref} is the reference voltage that is applied to the SVM module and V_{DC} is the DC voltage value.

This means that if the RSPWM modulation strategy is used, it requires at least double the reference voltage of the DC voltage to operate in the linear region. For the 380V phase-to-phase grid voltage system, the DC-link voltage after the second step can be calculated in (2):

$$V_{DC} = \sqrt{2}.V_{AC(L\text{-}L)} = \sqrt{2}.380 = 537(V) \quad (2)$$

Where: $V_{AC(L-L)}$ is the root-mean-square (RMS) phase to phase grid voltage.

The reference voltage that is applied to the SVM module can be determined from the phase-to-phase grid voltage in (3):

$$V_{ref} = \frac{\sqrt{2}.V_{AC(L\text{-}L)}}{\sqrt{3}} = \frac{\sqrt{2}.380}{\sqrt{3}} = 311(V) \quad (3)$$

Where: V_{ref} is the reference voltage that is applied to the SVM module.

It can be clearly seen that the DC-link voltage after the second step is lower than double the reference voltage, which is out of the linear modulation range of the RSPWM method. Stability problems may arise, and the controller will need to implement an anti-windup structure to adapt to this situation. Figure 5 shows the stability problem with the traditional approach when a low modulation index modulation strategy is used (RSPWM) and the effect of the anti-windup on the DC-link voltage response. Although this anti-windup structure can

help stabilize the system when the RSPWM modulation is working out of its linear modulation range, the voltage response fluctuates heavily around its reference value. A new ramp method must be proposed to overcome this problem and will be discussed in the next subsection.

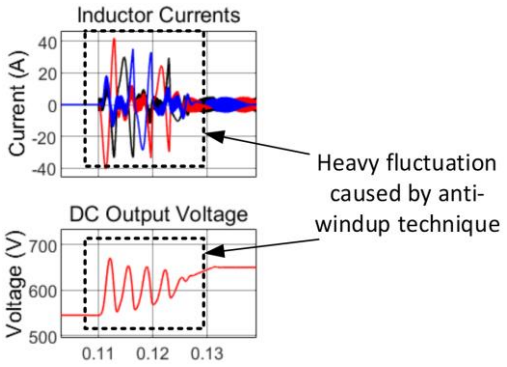

Figure 5: System response in the start-up procedure with RSPWM modulation method using Reference voltage ramp with anti-windup implementation.

2.4. Constant Duty Ramp

This method was developed from the duty cycle soft start method proposed in [13] but for the Three-Phase Three-Leg PFC. The same idea can be applied to a Three-Phase Four-Leg Inverter and achieve good start-up performance. However, the soft start duty cycle control also utilizes the calculated duty cycles from the control loop and for the same reason as the Reference Voltage Ramp, this method can't be used with a low modulation index modulation strategy. Note that the simulation results from Figure 6 are also taken from the test using the Conventional Three-Dimensional Space Vector PWM (SVM-3D) modulation technique.

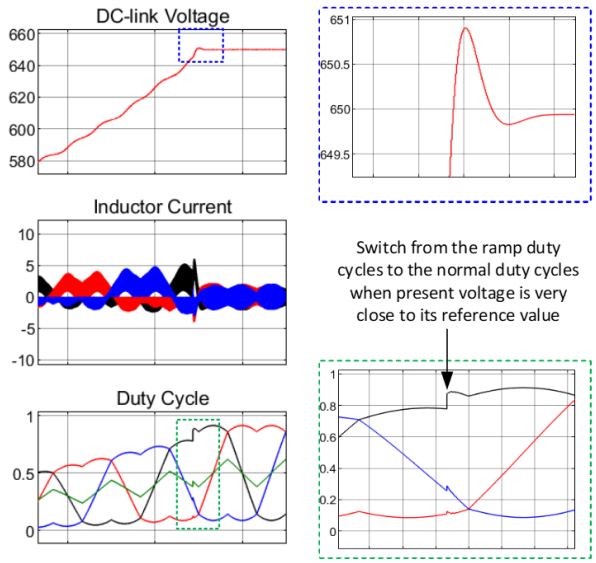

Figure 6: Matlab/Simulink simulation results with SVM-3D modulation strategy using the duty cycle soft start method.

The main difference between this Constant Duty Ramp method and the traditional Reference Voltage Ramp method comes in the use of the switching devices used in the start-up process. Instead of utilizing both the upper and lower switches in the start-up procedure, the Constant Duty Ramp method uses only the lower switches to charge the DC-link capacitor. All the lower switches are turned on with the same small duty while the upper ones are kept off until the end of the process. By applying this rule, when the lower switches are off, the inverter voltage v_{inva}, $v_{invb,}$ and v_{invc} in this interval are equal to the grid phase voltage v_{ga},$v_{gb,}$ and v_{gc}, respectively and there is no current through the filter inductors.

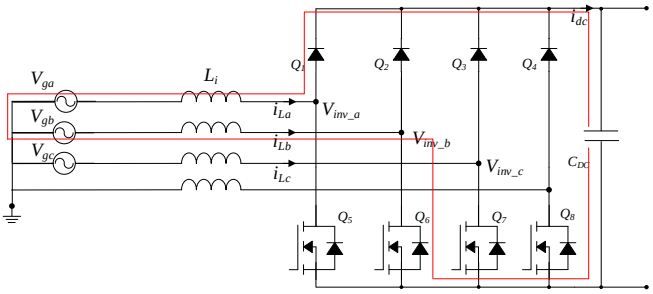

Figure 7: Current path for charging DC capacitor with the Constant Duty Ramp method.

When all the lower switches are turned on, as shown in Figure 8, the inverter voltages are clamped to zero, then the inductor current is generated which increases or decreases depending on the sign of each phase voltage at that moment. For example, in the analyzed interval in Fig. 8, v_{ga} is positive while v_{gb} and v_{gc} are negative, hence i_{La} is increasing while i_{Lb} and i_{Lc} are decreasing. However, at this moment, there is still no current through the body diode of switch Q_1 to charge the DC capacitor because this diode is in the reverse-biased state. After that, when the lower switches are turned off again, the diode of Q_1 is forward biased and the DC capacitor is charged slightly with the small charging current i_{dc} being equal to i_{La} as in Figure 8 and the current path being shown in Figure 7. When the inductor current i_{La} decreases to zero, the DC voltage stops increasing until the next turn-on signal for the lower switches.

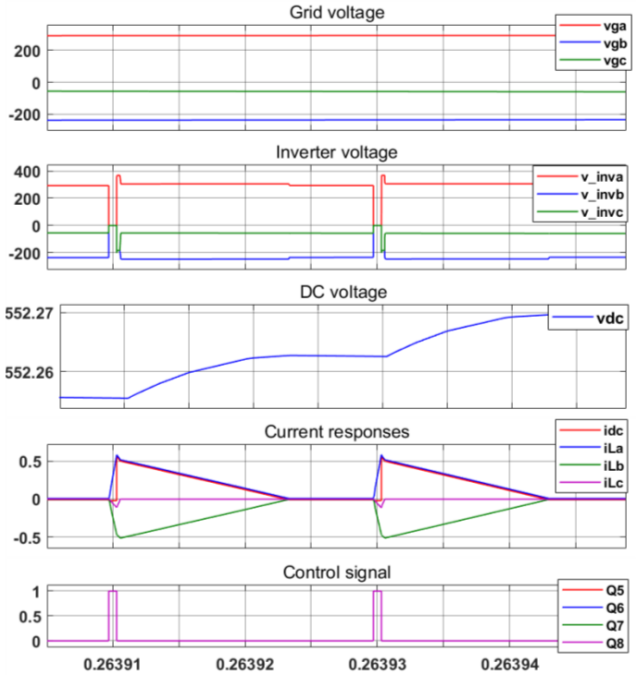

Figure 8: Key diagrams of the Constant Duty Ramp method

This method can be done only by applying constant duty cycles to the PWM so that the DC-link voltage will increase

gradually until the difference between it and the reference value is very small (just 1V for example). At this point, the lower switches will be enabled and the output voltage will be controlled to the reference value by applying the calculated duty cycles from the control loop.

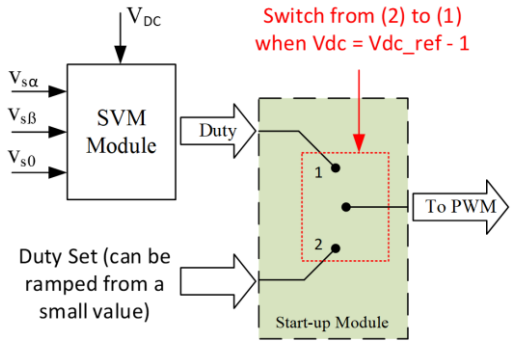

Figure 9: Constant duty ramp method block diagram

Since this method does not utilize the output duty cycles determined by the SVM module, the DC output voltage can increase to its reference value regardless of the modulation index of the modulation method used in the control structure. And thus it can overcome the problem that arises with the traditional reference DC voltage ramp approach. The constant duty ramp method is described via a block diagram in Figure 5. The constant duty cycles can be selected from a very small value to limit the inductor current at the start of step 3 (0.01 for example). However, too small a value can slow the process down and too large a value can result in big current spikes at the start of this stage. In order to both limit the PFC currents and enhance ramping procedure time, the duty cycles can be gradually increased from a small value to a large value instead of applying constant values as described in Figure 10.

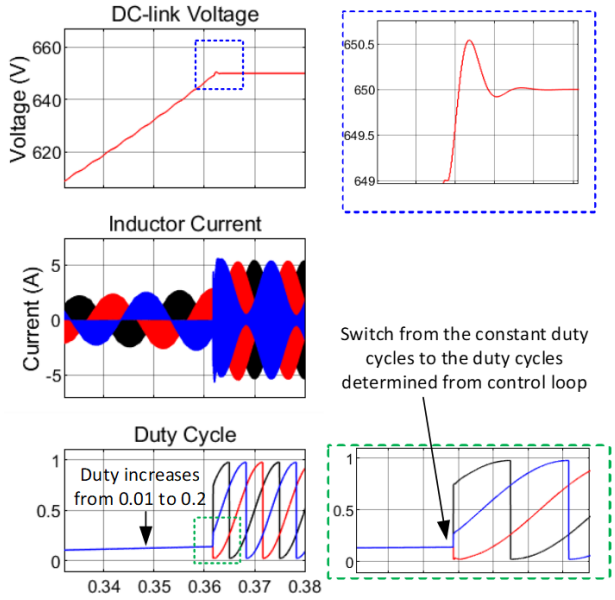

Figure 10: Simulation results of DC voltage, inductor currents, and duty cycles with the constant duty ramp method using the RSPWM modulation

Because of the ability to charge the DC capacitor without the need to concern about the modulation strategy used in the control loop, this method can be further used for different modulation strategies and/or different PFC topologies that require charging the bulk capacitor. A comparison between different start-up methods will be performed in the next section to show their strengths and weaknesses.

2.5. *Comparison of different start-up methods*

Simulations for different start-up methods with different PWM methods are carried out. The dynamic performances of voltage overshoot and current peak during the start-up procedure are compared and synthesized in Table 1. It can be clearly seen that while the RS-PWM method can not be started up with the Reference DC Voltage Ramp, the Constant Duty Ramp method is more viable than the other two methods due to its ability to charge the DC-link capacitor regardless of the modulation technique used in the control loop. Besides, this method introduces a similar current peak (5.2A and 4A) to the Reference Voltage Ramp method (3.6A). Furthermore, all three start-up methods can achieve neglectable voltage overshoot (around 0.5V – 1V), which ensures stability for the system to be ready for the next stage without faulting in the start-up process due to voltage and current clippings.

Table 1: Comparison between different start-up methods

	Reference DC Votlage Ramp		Constant Duty Ramp	
PWM method	SVM-3D	RS-PWM	SVM-3D	RS-PWM
Voltage Overshoot	1V	x	0.5V	0.5V
Peak current	3.6A	X	5.2A	4A

2.6. Hardware-in-the-loop Experimental

The proposed start-up procedure has been applied to a system with a rated voltage of 380 V_rms (line-line), rated power of 11kW, and DC output voltage of 650V. The Over-current protection level (OCP) in this research is selected at 20A, which is higher than the nominal phase current of 16.67A. The Over-Voltage Protection (OVP) level is selected at 700V for practical purposes.

Table 2: Main design parameters

Parameters	Value	Unit
Nominal Power	11	kW
Grid voltage (L-L)	380	V
Grid frequency	50	Hz
DC Output Voltage	650	V
Switching frequency	50	kHz
L filter	350	µH
DC-link capacitor	1000	µF
Precharge resistor	50	Ω
Over-Voltage Protection (OVP)	700	V
Over-Current Protection (OCP)	20	A

In order to illustrate the proposed start-up procedure, a Hardware-in-the-loop experiment is carried out using Typhoon HIL 402. Typhoon HIL is the real-time Hardware-in-the-loop platform for the design, testing, and validation of power electronics systems, which helps reduce the cost of testing and improve quality and reliability. This is used as a power circuit simulator which shows the system response when being controlled by digital controllers. The control loop is done via DSP C2000 TMS320F28379D from Texas Instrument (TI). The two devices are connected using a board connector that wired every PWM output pin from the TMS320F28379D development kit to the Digital Inputs (DI) of the Typhoon HIL and every ADCIN input pin from TMS320F28379D to the Analog Outputs (AO) of the Typhoon HIL. The pin configuration of

the DSP controller and the Typhoon HIL are shown in Figure 9 to describe how the experiment is carried out.

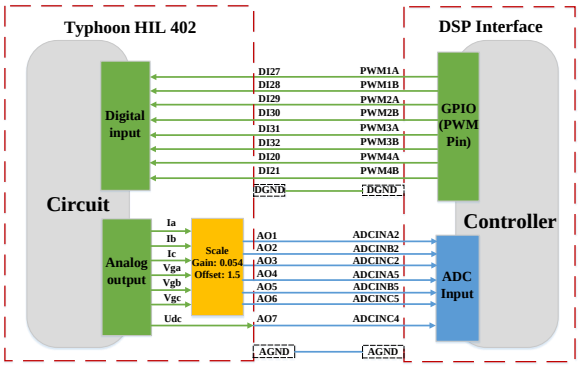

Figure 11: Pin configuration in the experiment setup

To better understand the pros and cons of each start-up method, four independent experiments are performed. Two of them are implemented with the reference voltage ramp start-up method using a high modulation index modulation strategy (SVM-3D) and a low modulation index modulation technique (RSPWM). The rest two cases are tested with the constant duty ramp method using the same modulation techniques as the first two cases. The results of all test scenarios are shown in Figure 12 and Figure 13. As can be seen from Figure 12a and Figure 12b, the case with the SVM-3D method shows great results: Low DC output voltage overshoot is less than 1V which meets the OCV standard, and low start-up currents (around 4A) that is under the OCP level during the start-up procedure.

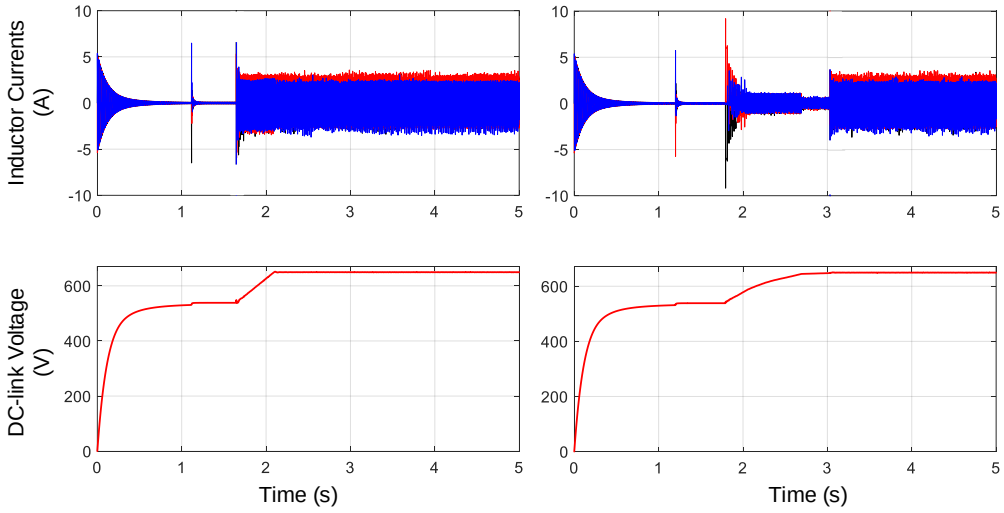

Figure 12: Experimental results. a) Reference voltage ramp with SVM-3D, b) Constant duty ramp with SVM-3D

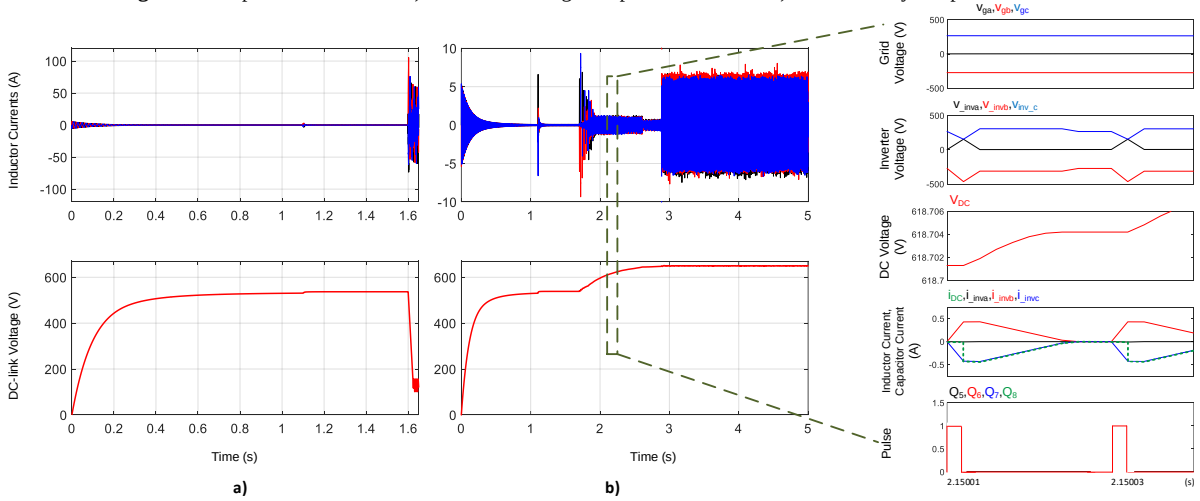

Figure 13: Experimental results. a) Reference voltage ramp with RSPWM; b) Constant duty ramp with RSPWM

However, the case with the RSPWM method shows the opposite. It is very clear from Figure 13a that the system is unstable with a peak current of around 100A and a sudden decrease of the DC voltage. This problem occurs because the DC-link voltage after the second step is not enough for the RSPWM method operating in the linear modulation range with the detailed equation presented in section 2.3. The controller then works unstably and the output of the DC voltage controller is quickly saturated, leading to high spikes and fluctuation in the output currents, which shows good agreement with the Matlab/Simulink simulation results.

Figure 12b and Figure 13b illustrate that the constant duty ramp start-up method is well adapted to both modulation techniques. The key diagram of this method with the RS-PWM method is similar to the theoretical analysis in section 3.2. This method utilizes constant duty cycles to ramp up the DC-

link voltage until it almost reaches the reference value, which ensures the RSPWM method performs within its linear modulation range. Although this method solved the problem with the traditional start-up approach, it introduced unwanted current peaks (around 6A) in the switching stage from the constant duty cycles to the duty cycles calculated from the control loop. It comes to the conclusion that if a high modulation index modulation strategy is used in the control loop, the reference voltage ramp method should be used due to its better current dynamic responses but if a low modulation index modulation method is used, the constant duty ramp should be prioritized due to its ability to ensure enough DC voltage for the system to operate normally.

3. Conclusion

In this paper, a three-step start-up procedure for a three-phase four-leg inverter in grid-connected mode is proposed. This procedure ensures that the inrush currents stay below the Over Current Protection (OCP) level and the output voltage increases to the reference value with a small overshoot. The reference voltage ramp method is introduced first to show the traditional approach to control the DC voltage to its reference value. However, this method has difficulty to apply for low modulation index modulation strategies such as RSPWM. The proposed start-up method, constant ramp duty, ensures enough DC voltage for the modulation to perform in its linear modulation range and helps stabilize the system without any complicated changes in the control loop. Hardware-in-the-loop experimental results using Typhoon HIL 402 and DSP TMS320F28379D also show good agreement with the theoretical analysis and the Matlab/Simulink simulation results, which improves the feasibility of future experiments.

Acknowledgment

Tuan Anh Do was funded by the Master, PhD Scholarship Programme of Vingroup Innovation Foundation (VINIF), code VINIF.2022.TS002.

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