A Novel Active Quasi Z-Source Multilevel Inverter with Capacitor Voltage Reduction

Duc Tri Do[1], Bich Nga Truong Thi[1], Vinh Thanh Tran[1], Anh Tuan Nguyen Phan[1]*

[1] *Ho Chi Minh City University of Technology and Education*
[*]*Corresponding author E-mail: nguyenphananhtuan15447@gmail.com*

Abstract

This paper presents an active Z-source multilevel inverter that incorporates an additional semiconductor switch and diode into the impedance-source network to enhance voltage gain. The integration of these components into the Z-source network significantly reduces the voltage stress on the inverter components, as demonstrated through comparisons with previous studies. The innovative topology features two key elements: an AqZS, which improves the inverter's voltage gain, and a three-level T-type inverter at the forefront. The shoot-through signal is integrated into the operating state of the three-level T-type inverter, enabling control of the input voltage on the appropriate side of the inverter. This is achieved by charging and discharging components in the reactive source network, resulting in a high voltage gain. The paper introduces the discontinuous pulse width modulation (DPWM) technique to control the inverter. This control method combined with ST state ensures no additional switching compared to other conventional inverters. To highlight the contributions of this paper, a detailed analysis of the steady-state operational principles of the proposed topology and its control method is presented. Furthermore, simulation and experimental results are provided to validate the accuracy and effectiveness of the proposed topology and method.

***Keywords**: T-type Inverter, Impedance Source Network, Active quasi-Z Source inverter, DPWM*

Symbols

Symbols	Units	Description
C_{1N} and C_{2N}	F	The lower capacitors of AqZS
C_{1P} and C_{2P}	F	The upper capacitors of AqZS
L_{1N} and L_{2N}	H	The lower inductors of AqZS
L_{1P} and L_{2P}	H	The upper inductors of AqZS

Abbreviations

3L-AqZS-T^{2}I	Three-level Active quasi Z-source
AqZS	Active quasi Z-source
DPWM	Discontinuous pulse width modulation
ZSI	Z-Source Inverter
q-ZSI	quasi Z-source Inverter
NST	Non Shoot-through
ST	Shoot-through

Tóm tắt

Bài báo này trình bày một bộ nghịch lưu đa bậc nguồn Z tích cực, tích hợp thêm một khóa bán dẫn và diode vào mạng nguồn kháng với mục đích tăng cường độ lợi điện áp. Việc thêm diode và khoá tích cực vào mạng nguồn Z giúp điện áp đặt trên các linh kiện trong bộ nghịch lưu giảm đáng kể, điều này được minh chứng thông qua so sánh với các nghiên cứu trước đó. Cấu trúc đề xuất bao gồm hai thành phần chính: một nguồn Z tích cực để nâng cao độ lợi điện áp của hệ thống và một mạch nghịch lưu ba pha ba bậc hình T. Tín hiệu ST được chèn vào trạng thái hoạt động của bộ nghịch lưu ba pha ba bậc hình T. Điều này cho phép điều khiển điện áp đầu vào ở phía mạch nghịch lưu thích hợp bằng cách nạp và xả các thành phần trên phía mạng nguồn kháng, mang lại độ lợi điện áp cao. Bài báo này đề xuất một phương pháp điều chế DPWM để điều khiển bộ nghịch lưu, phương pháp này giúp giảm hiệu quả số lần chuyển mạch so với các chiến lược điều khiển truyền thống. Bằng cách áp dụng phương pháp này, việc thêm trạng thái ST không dẫn đến bất kỳ lần chuyển mạch bổ sung nào. Để làm nổi bật sự đóng góp của bài báo, việc phân tích nguyên lý hoạt động của cấu hình đề xuất ở trạng thái ổn định, phương pháp điều khiển được trình bày cụ thể. Ngoài ra, kết quả mô phỏng và thí nghiệm sẽ được trình bày để xác minh tính đúng đắn của cấu hình và phương pháp đề xuất.

1. Introduction

Voltage source inverters (VSIs) have gained widespread use in contemporary industrial applications, including electric vehicles, renewable energy systems, energy storage systems, and motor control [1-3]. Choosing the appropriate topology for these applications is crucial, taking into account various factors such as superior efficiency, streamlined design, and cost reduction. In this research, the implementation of a multilevel inverter is presented as a promising approach to fulfill these requirements.

The T-type inverter stands out as a highly promising topology among various inverter designs, providing notable advantages compared to other types of inverters. Due to its capacity for achieving high energy conversion efficiency and enhancing power quality, this converter has become increasingly popular in automotive and photovoltaic (PV) systems [4]. Unlike the conventional three-level neutral point clamped (NPC) inverter, the T-type inverter utilizes two active neutral-point switches linked to the DC-link voltage neutral point [5], thus significantly reducing the number of diodes [6]. With this structure leads to reduced power losses in the medium-range

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power and a more compact implementation. Additionally, each bidirectional switch connected to the DC-link neutral point only needs to withstand half of the DC-link voltage, enabling the use of lower-voltage power devices [7]. Researchers are increasingly focused on developing inverters capable of managing a wide range of input voltages. Nonetheless, VSI inverters are not intrinsically configured to support such extensive input voltage ranges [8]. A common approach to addressing this issue involves incorporating a DC-DC boost converter ahead of the VSI side, thus facilitating voltage elevation within a two-stage power conversion framework. This setup increases the input voltage before it enters the inverter side.

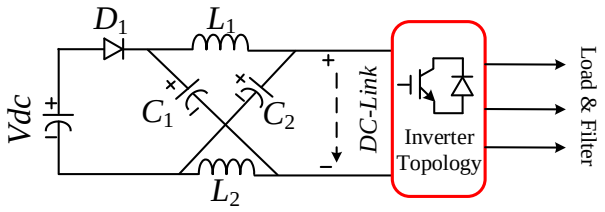

Figure 1: The Z-Source impedance network topology.

To tackle these challenges, F.Z. Peng introduced the Z-Source Inverter (ZSI) in 2003 as an innovative approach that utilizes impedance networks. The ZSI is characterized by an X-shaped configuration comprising two inductors and two capacitors [9]. Figure 1 illustrates the topology of the Z-Source impedance network. Despite its advantages, the ZSI encountered certain drawbacks, such as discontinuous input current, higher initial current surges, elevated voltage stress on capacitors, and larger component sizes. To address these limitations, the quasi-Z Source Inverter (q-ZSI) was developed. The q-ZSI retained the benefits of the original ZSI but employed a different configuration with passive power components like inductors (L) and capacitors (C). The q-ZSI's key features include continuous DC input current, reduced voltage stress on capacitors, and more compact component sizes. These enhancements make the q-ZSI a viable solution for overcoming the shortcomings of conventional voltage source inverters [10].

A reduced duty ratio leads to a decreased current ripple in the inductor, which allows for a smaller inductor size and boosts the power density of the inverter [10]. However, introducing the shoot-through state substantially increases the number of switching times. In inserting the ST state, traditional approaches for impedance-source inverters typically add at least two commutations. These extra commutations result in higher switching losses in switches. As a result, many studies have focused on developing techniques to minimize switching commutations and reduce the ST duty ratio [12].

This paper presents a new active impedance source by integrating an additional switch and diode into the existing q-ZSI, which is referred to as the AqZSI. To mitigate switching commutations and enhance efficiency in the T-type three-level inverter system, the DPWM algorithm is utilized. By altering the number of voltage levels, the requisite impedance must be added in multiples of (n-1), where n represents the total number of levels and is an odd integer. This research will offer theoretical analysis and simulation outcomes to validate the efficacy of the proposed approach.

2. Three Phase Three-Level Active quasi-Z Source T-Type Inverter

The 3L-AqZS-T^{2}I topology shown in Figure 2 consists of an AqZS impedance network, a conventional three phase three-level T-type inverter circuit, a load, and a low-pass filter. The AqZS impedance network includes 4 inductors (L_{1P}, L_{2P}, L_{1N}, L_{2N}), 4 capacitors (C_{1P}, C_{2P}, C_{1N}, C_{2N}), 4 diodes (D_{1P}, D_{2P}, D_{1N}, D_{2N}), and two semiconductor switches (S_P and S_N). Compared to the conventional qZSI topology, the proposed design adds an extra semiconductor switch and a diode.

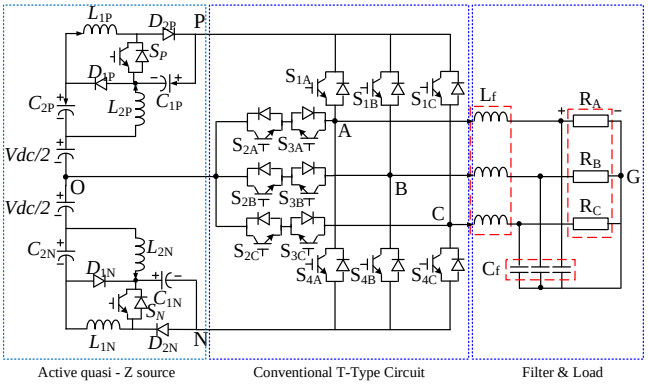

Figure 2: The topology of 3L-AqZS-T^{2}I.

This addition enhances the flexibility of the system in controlling the boost factor and the voltage gain of the inverter. The conventional three phase three-level T-type inverter operates under a buck mode from a fixed DC-Link source, with each phase leg of the inverter comprising 4 semiconductor switches S_{1X}, S_{2X}, S_{3X}, and S_{4X} (where X = A, B, C), ensuring three output voltage levels of $+V_{PN/2}$, 0, $-V_{PN/2}$.

2.1. Operating States

Just like any of the single-stage inverters, 3L-AqZS-T^{2}I has also been developed to work in the ST mode and in the NST mode, as shown in Figure 3. The operating status of the semiconductors is detailedly presented in Table 1.

The states of the 3L-AqZS-T^{2}I as produced in three states are shown in Figure 3 and referred to as NST1, NST2, and ST. In the ST mode, as depicted in Figure 3(a), all the power switches on at least one phase leg of the inverter are turned on, and semiconductor devices S_P, S_N in the AqZS side are deactivated. Diodes D_{1P}, D_{1N} are reverse-biased, while diodes D_{2P} and D_{2N} are forward-biased.

In this mode, inductors L_{1P} and L_{1N} store energy from the input voltage $V_{dc/2}$, capacitor C_{2P}, and capacitor C_{2N}, while inductors L_{2P} and L_{2N} store energy from the input voltage $V_{dc/2}$, capacitor C_{1P}, and capacitor C_{1N}. The inductors voltage V_{L2P}, V_{L1P}, V_{L1N}, V_{L2N} and the current capacitors i_{C1P}, i_{C2P}, i_{C1N}, i_{C2N} expressed as follows:

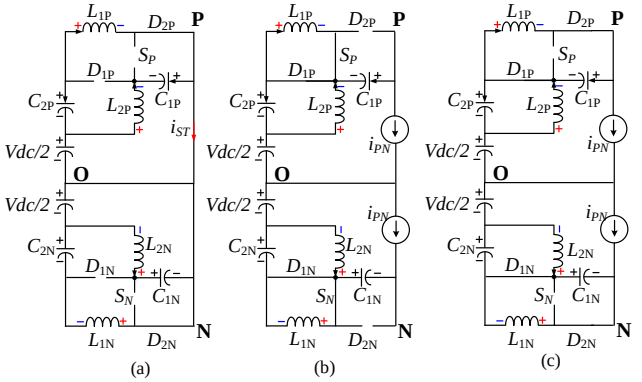

Figure 3: Operating mode of 3L-AqZS-T^{2}I. (a) ST mode, (b) NST1 mode, (c) NST2 mode.

Table 1: On/ Off states of 3L-AqZS-T^{2}I, **(**In which, X can be A, B or C).

Mode	ON Switch	ON Diode	V*xo*
ST	S_{1X}, S_{2X}, S_{3X}, S_{4X}	D_{2P}, D_{2N}	*0*
NST1	S_P,S_N S_{1X}, S_{2X}/ S_{2X},S_{3X}/ S_{3X}, S_{4X}	D_{1P}, D_{1N}	$+V_{dc/2}$, *0*, or $-V_{dc/2}$
NST2	S_{1X}, S_{2X}/ S_{2X},S_{3X}/ S_{3X}, S_{4X}	D_{1P}, D_{1N}, D_{2P}, D_{2N}	$+V_{dc/2}$, *0*, or $-V_{dc/2}$

$$\begin{cases} L_{1P}\dfrac{di_{L1P}}{dt}=\dfrac{V_{dc}}{2}+V_{C2P}; & L_{2P}\dfrac{di_{L2P}}{dt}=\dfrac{V_{dc}}{2}+V_{C1P} \\ C_{1P}\dfrac{dv_{C1P}}{dt}=-i_{L2P}; & C_{2P}\dfrac{dv_{C2P}}{dt}=-i_{L1P} \end{cases} \quad (1)$$

$$\begin{cases} L_{1N}\dfrac{di_{L1N}}{dt}=\dfrac{V_{dc}}{2}+V_{C2N}; & L_{2N}\dfrac{di_{L2N}}{dt}=\dfrac{V_{dc}}{2}+V_{C1N} \\ C_{1N}\dfrac{dv_{C1N}}{dt}=-i_{L2N}; & C_{2N}\dfrac{dv_{C2N}}{dt}=-i_{L1N} \end{cases} \quad (2)$$

In the NST1 state, switches S_P and S_N are activated, diodes D_{2P} and D_{2N} are non-conducting, while diodes D_{1P} and D_{1N} are conductive as shown in Table 1.

$$\begin{cases} L_{1P}\dfrac{di_{L1P}}{dt}=0; L_{2P}\dfrac{di_{L2P}}{dt}=-V_{C2P} \\ C_{1P}\dfrac{dv_{C1P}}{dt}=-i_{PN}; C_{2P}\dfrac{dv_{C2P}}{dt}=i_{L2P}-i_{PN} \end{cases} \quad (3)$$

$$\begin{cases} L_{1N}\dfrac{di_{L1N}}{dt}=0; L_{2N}\dfrac{di_{L2N}}{dt}=-V_{C2N} \\ C_{1N}\dfrac{dv_{C1N}}{dt}=-i_{PN}; C_{2N}\dfrac{dv_{C2P}}{dt}=i_{L2N}-i_{PN} \end{cases} \quad (4)$$

In this operating mode, inductors L_{1P} and L_{1N} are short-circuited, and capacitors C_{1P} and C_{1N} discharge their stored energy. During this time, capacitor C_{2P} is charged by inductor L_{2P}, and capacitor C_{2N} is charged by inductor L_{2N}. The NST1 state is illustrated in Figure 3(b).

In NST2, switches S_P and S_N are turned off, and the circuit operates similarly to T-type inverter. All diodes in the AqZS side are conductive. Figure 3(c) illustrates the NST2 mode. The output pole voltages V_{XO} are shown in Table 1.

$$\begin{cases} L_{1P}\dfrac{di_{L1P}}{dt}=-V_{C1P}; & L_{2P}\dfrac{di_{L2P}}{dt}=-V_{C2P} \\ C_{1P}\dfrac{dv_{C1P}}{dt}=i_{L1P}-i_{PN}; & C_{2P}\dfrac{dv_{C2P}}{dt}=i_{L2P}-i_{PN} \end{cases} \quad (5)$$

$$\begin{cases} L_{1N}\dfrac{di_{L1N}}{dt}=-V_{C1N}; & L_{2N}\dfrac{di_{L2N}}{dt}=-V_{C2N} \\ C_{1N}\dfrac{dv_{C1N}}{dt}=i_{L1N}-i_{PN}; & C_{2N}\dfrac{dv_{C2N}}{dt}=i_{L2N}-i_{PN} \end{cases} \quad (6)$$

2.2. DPWM Scheme

To lower switching losses and encourage three-phase VSI effectiveness of three-phase voltage source inverters, the Discontinuous Pulse-Width Modulation (DPWM) algorithm has been proposed. This technique helps decrease the on/off switching losses of power switches compared to traditional sine-PWM control method. As a result, it enhances the lifespan of semiconductor switches, reduces cooling costs, and raises the inverter circuit's power density. Additionally, the DPWM method reduces the number of switching events by 33% and increases the voltage gain to nearly 1.15 compared to conventional sine-PWM method. In order to give a thorough explanation of this modulation technique, consider the following three signals, $V_{ref\,X}$ ($X = A$, B, and C):

$$\begin{cases} V_k = \frac{1}{6}[\sin(3\omega t)] \\ V_{ref_A} = \frac{2}{\sqrt{3}}[M\sin(\omega t)]+V_k \\ V_{ref_B} = \frac{2}{\sqrt{3}}[M\sin(\omega t-2\pi/3)]+V_k \\ V_{ref_C} = \frac{2}{\sqrt{3}}[M\sin(\omega t+2\pi/3)]+V_k \end{cases} \quad (7)$$

Where: M is modulation index ($M \le 1$).

By using equation (8), the reference voltages in equation (7) will be re-modulated.

$$\begin{cases} V^{*P}_{ref_A} = V_{refA} * (V_{refA} > 0) \\ V^{*P}_{ref_B} = V_{refB} * (V_{refB} > 0) \\ V^{*P}_{ref_C} = V_{refC} * (V_{refC} > 0) \end{cases} \quad (8)$$

Reference voltages V^{*N}_{refA}, V^{*N}_{refB}, V^{*N}_{refC} are obtained by shifting the reference voltages V^{*P}_{refA}, V^{*P}_{refB}, V^{*P}_{refC} by 180 degrees respectively.

V_{ST} is defined as the sum of the maximum values of the six reference signals and d, which are used to compare with the carrier to generate the transmitted state.

$$V_{ST} = f_{\max}(V^{*P}_{refA}, V^{*P}_{refB}, V^{*P}_{refC}, V^{*N}_{refA}, V^{*N}_{refB}, V^{*N}_{refC}) + d \quad (9)$$

Where: ($0 < d \le 1-M$) represents the shoot-through ratio.

The ST signal for the inverter leg is produced by a continuous signal in the traditional PWM control scheme for single-stage inverters.

$$f_{\max}(V^{*P}_{refA}, V^{*P}_{refB}, V^{*P}_{refC}, V^{*N}_{refA}, V^{*N}_{refB}, V^{*N}_{refC}) \le V_{tri} \le V_{ST}.$$

In the ST mode, S_{1X}, S_{2X}, S_{3X}, S_{4X} on the inverter side are gated on. The control signal V_{con}, which provides the gating pulses for the two switches S_P and S_N, is defined as follows:

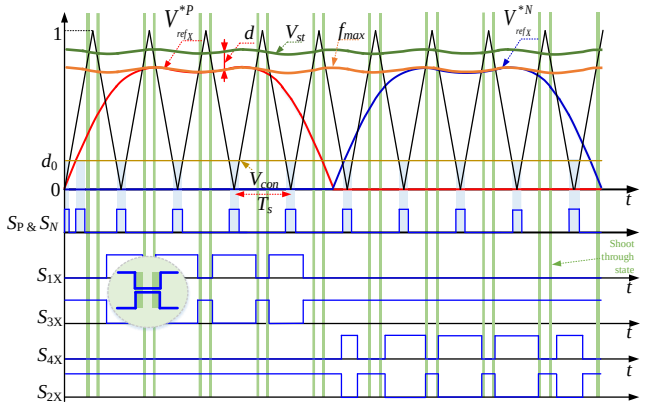

Figure 4: The reference waveform of the DPWM control technique for the 3L-AqZS-T^{2}I inverter.

$$V_{con} = d_0 \tag{10}$$

Where: d_o carries out the S_P and S_N switch duty cycle. In order to guarantee consistent system performance, the value of V_{con} needs to fulfill the subsequent criteria:

$$\begin{aligned} &V_{con} \le Min[f_{\max}(V^{*P}_{refA}, V^{*P}_{refB}, V^{*P}_{refC}, V^{*N}_{refA}, V^{*N}_{refB}, V^{*N}_{refC})] \\ &\Leftrightarrow d_0 \le Min[f_{\max}(V^{*P}_{refA}, V^{*P}_{refB}, V^{*P}_{refC}, V^{*N}_{refA}, V^{*N}_{refB}, V^{*N}_{refC})] \end{aligned} \tag{11}$$

All the reference signals presented above will be compared with the carrier wave at high frequency to generate control pulse signals for the power electronic semiconductor switches of the system. This comparison is presented clearly and specifically in Figure 4.

2.3. Steady-State Analysis

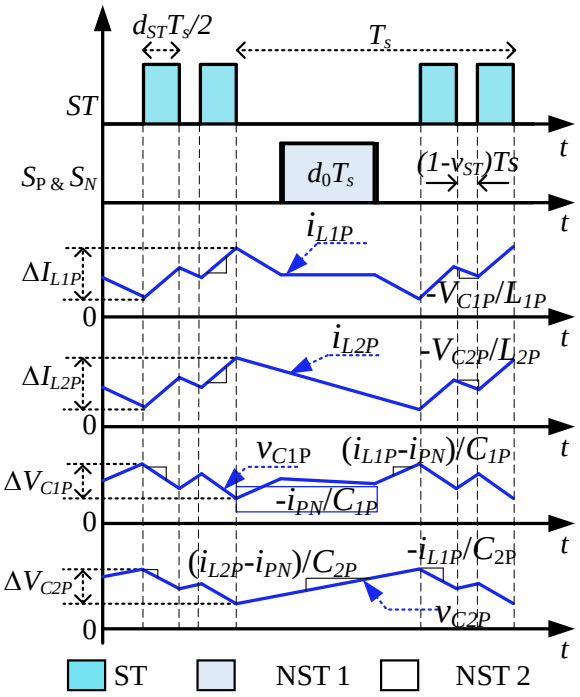

Figure 5: The capacitor voltage and inductor current waveform on the AqZS side during one switching cycle.

Based on the operating principles and control method presented, the voltages across C_{1P}, C_{2P}, C_{1N}, and C_{2N} are listed in the following order:

$$V_{C1P} = V_{C1N} = \frac{(V_{dc}/2).d}{1-d_0-2d+d.d_0} \tag{12}$$

$$V_{C2P} = V_{C2N} = \frac{(V_{dc}/2).d.(1-d_0)}{1-d_0-2d+d.d_0} \tag{13}$$

From equations (12) and (13), the DC-link voltage (V_{PN}) is determined as follows:

$$\begin{aligned} &V_{PN} = (V_{C1P}+V_{C2P}+V_{dc/2})+(V_{C1N}+V_{C2N}+V_{dc/2}) \\ &\Rightarrow V_{PN} = \frac{V_{dc}(1-d_0)}{1-d_0-2d+d.d_0} \end{aligned} \tag{14}$$

Applying the charge balance concept to the capacitors for the currents through C_{1P}, C_{2P}, C_{1N}, and C_{2N} will approximate the average values of the inductor currents, assuming that the inverter's (i_{PN}) current is constant.

$$\begin{cases} I_{L1P} = i_{PN}(1-d)/(1-d_0-2d+d_0.d) \\ I_{L2P} = i_{PN}(1-d_0)(1-d)/(1-d_0-2d+d_0.d) \end{cases} \tag{15}$$

$$\begin{cases} I_{L1N} = i_{PN}(1-d)/(1-d_0-2d+d_0.d) \\ I_{L2N} = i_{PN}(1-d_0)(1-d)/(1-d_0-2d+d_0.d) \end{cases} \tag{16}$$

The boost factor, (B), of the inverter is calculated using Equation (15) and (16):

$$B = \frac{V_{PN}}{V_{dc}} = \frac{1-d_0}{1-d_0-d(2-d_0)} \tag{17}$$

Based on the modulation index M and the boost factor B, the peak amplitude of the fundamental component of the output voltage is computed as follows:

$$\hat{V}_x = \frac{1}{\sqrt{3}} M.V_{PN} \tag{18}$$

The voltage gain G of the proposed 3L-AqZS-T^{2}I inverter is expressed as:

$$G = \frac{2\hat{V}_X}{V_{dc}} \tag{19}$$

3. Three-Phase 3L-AqZS-T^{2}I

3.1. Inductor and Capacitor selection

Figure 5 shows the capacitor voltage and inductor current waveforms in AqZS side. It can be observed that the current ripple in the inductor depends on duration of NST 2 mode, (1-*Vst*).T_s .

When V_{st} is at its maximum, the current ripple through the inductor reaches its peak value. Based on Equation (9), the maximum value of V_{st} is calculated as follows:

$$V_{ST-\max} = M + d \tag{20}$$

According to equations (1) through (6) and (20), the maximum value of the current ripple through the inductor is calculated as follows:

Table 2. Comparison of Components Between the Proposed Inverter and Previous Studies

	qSBT^{2}I [15]	3L-qSBFTI [16]	RC^2-AIS [17]	ADC-qZSI [18]	Proposed AqZSI
Inductor current ripple	$\frac{V_{dc}}{2L_i}d_0T$	$\frac{2d(1-d).V_{dc}.T}{L_B(1-2d)}$	$\frac{2d(1-d).V_{dc}.T}{L_B(1-2d)}$	$\frac{V_{dc}M(1-d_0)T}{L_1(1-d_0-2d+d.d_0)}$ $\frac{V_{dc}d(M-d_0)T}{L_2(1-d_0-2d+d.d_0)}$	$\frac{V_{dc}d(M-d_0)T}{2L_{1P}(1-d_0-2d+d.d_0)}$ $\frac{V_{dc}M(1-d_0)T}{2L_{2P}(1-d_0-2d+d.d_0)}$
Capacitor voltage stress, V_C/V_{dc}	$\frac{1}{1-2d_0}$	B/2	$\frac{1}{1-2d}$	dB, C_1 ; $\frac{d}{1-d_0}B, C_2$	$\frac{d}{2.(1-d_0)}, C_{1P}$; $\frac{d.B}{2}, C_{2P}$
Diode voltage stress, V_D/V_{dc}	NA	B/2	$\frac{1}{1-2d}$	B, D_1 ; $\frac{d}{1-d_0}B, D_2$	$\frac{d}{2.(1-d_0)}, D_{1P}$; $\frac{B}{2}, D_{2P}$
Switch voltage stress, V_S/V_{dc}	$\frac{1}{1-2d_0}$	B/2	$\frac{1}{1-2d}$	$\frac{d}{1-d_0}B$	$\frac{d}{2.(1-d_0)}B$
Inductors	1	1	1	2	4
Capacitors	2	2	2	2	4
Diodes	4	3	2	2	4
Switches	2	2	1	1	2
Output voltage	3-level	3-level	3-level	2-level	3-level

$$\begin{cases} \Delta I_{L1P} = \frac{V_{dc}}{2} d(M-d_0)/(KL_{1P}f_s) \\ \Delta I_{L2P} = \frac{V_{dc}}{2} M(1-d_0)/(KL_{2P}f_s) \\ K = 1-d_0-2d+d_0d \end{cases} \quad (21)$$

$$\begin{cases} \Delta I_{L1N} = \frac{V_{dc}}{2} d(M-d_0)/(KL_{1N}f_s) \\ \Delta I_{L2N} = \frac{V_{dc}}{2} M(1-d_0)/(KL_{2N}f_s) \\ K = 1-d_0-2d+d_0d \end{cases} \quad (22)$$

Where ΔI_{LjP} (j=1,2) and ΔI_{LjN} (j=1,2) respectively, are the current ripples through the inductor on the upper and lower sides of the impedance network, $f_s=1/T_s$ is the switching frequency.

The voltage ripple across the capacitor is determined as:

$$\begin{cases} \Delta V_{C1P} = i_{PN}[Md-(K-d)d_0]/(KC_{1P}f_s) \\ \Delta V_{C2P} = i_{PN}Md/(KC_{2P}f_s) \end{cases} \quad (23)$$

$$\begin{cases} \Delta V_{C1N} = i_{PN}[Md-(K-d)d_0]/(KC_{1N}f_s) \\ \Delta V_{C2N} = i_{PN}Md/(KC_{2N}f_s) \end{cases} \quad (24)$$

Where ΔV_{CjP} (j=1,2) and ΔV_{CjN} (j=1,2) are the voltage ripples across the capacitors on the upper and lower sides of the impedance network respectively. Based on Equations (12) – (16) and (21) – (24), the inductors and capacitors in the AqZS circuit are selected according to the conditions $\Delta I_{Lj}/I_{Lj} \le k_1\%$, and $\Delta V_{Cj}/V_{Cj} \le k_2\%$, where $k_1\%$ and $k_2\%$ are the maximum allowable ripple ratios for the inductor current and capacitor voltage ripple, respectively.

3.2. Switches and Diodes Selection

The maximum reverse voltage of diodes D_{1P} and D_{1N} is half the DC-link voltage (V_{dc}/2) during the ST mode. The maximum reverse voltage of diodes D_{2P} and D_{2N} equals the voltage across capacitors C_{1P} and C_{1N}, respectively, during non-shoot-through mode 1 (NST 1).

The maximum current through diodes D_{2P} and D_{2N} is equal to the maximum current through inductors L_{1P} and L_{1N}, respectively, during non-shoot-through mode 2 (NST2). Meanwhile, the maximum current through diodes D_{1P} and D_{1N} during non-shoot-through modes is calculated as follows:

$$\begin{cases} i_{D1P,\max} = i_{L1P,\max} + i_{L2P,\max} - i_{PN} \\ i_{D1N,\max} = i_{L1N,\max} + i_{L2N,\max} - i_{PN} \end{cases} \quad (25)$$

$$\begin{cases} i_{LjP,\max} = I_{LjP} + \Delta I_{LjP}/2 \\ i_{LjN,\max} = I_{LjN} + \Delta I_{LjN}/2 \end{cases} \quad (j=1,2) \quad (26)$$

Where $i_{LjP,max}$ và $i_{LjN,max}$ are the maximum current values through inductors L_{jP} and L_{jN}, respectively, as presented through Equations (15) – (16) and (21) – (22).

The switches S_P and S_N are responsible for transferring energy from inductors L_{1P} and L_{1N}. When S_P and S_N are activated, the current through inductors L_{1P} and L_{1N} remains constant, as shown in the waveform of Figure 5. Therefore, the current

through the two semiconductor switches S_P and S_N is the average value of the currents through L_{1P} and L_{1N}, as expressed in Equations (15) and (16).

The voltage stress to switches S_P and S_N is the voltage across capacitors C_{1P} and C_{1N}, respectively. The voltage stress to the two switches in the half-bridge configuration, S_{1X} and S_{4X}, is the DC-link voltage, while the voltage stress to the two bidirectional switches, S_{2X} and S_{3X}, is half the DC-link voltage (V_{PN}/2).

3.3. Component Voltage Rating

The main strengths of the proposed topology are using fewer passive components and high voltage gain. Although using more electronic components than studies [15-17], the outstanding point of the proposed AqZSI configuration is reducing voltage stress on electronic components. This helps reduce system costs, especially the cost of power electronic devices. In addition, the voltage stress on the capacitors of the proposed configuration is very low, which helps increase the power density of the circuit. In this section, a comparison of voltage stress on components will be performed to clarify the strengths of the proposed topology.

$$B = G / (1.15 \times M) \quad (27)$$

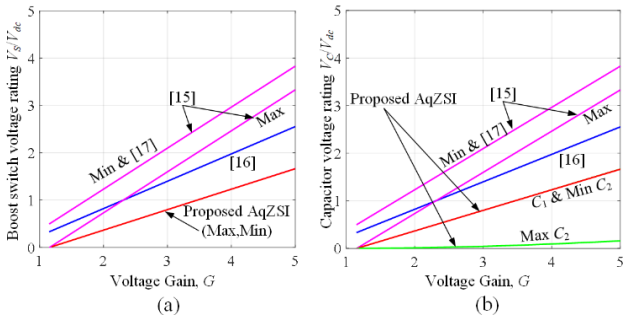

Figure 6. Comparison about component voltage rating: (a) voltage gain vs capacitor, (b) voltage gain vs boost switch

The coefficients d and d_0 presented in formulas (9) and (11) are the main factors controlling the boost factor B. Therefore, in this comparison, the indices d and d_0 are controlled in both maximum boost control and minimum boost control conditions. In the maximum boost control condition, the coefficient d_0 is set to the minimum value of the function fmax presented through formula (11), on the contrary, in the minimum boost control condition, the coefficient d0 is set to zero. The duty ratio ST or D_{ST} or d, in the studies, is set to (1-M). Figures 6(a) and (b) show the voltage gain and capacitor and voltage gain and boost switch of the previous studies and the proposed configuration, respectively.

From Table 2, the proposed AqZSI topology incorporates more components than topologies [15] – [18]. Specifically, it uses 3 additional inductors compared to topologies [15] – [17], 2 additional inductors compared to [18], and 2 additional capacitors compared to [15] – [18]. Additionally, it employs 1 more diode than topology [16] and 2 more diodes than [17] and [18]. Furthermore, the proposed inverter, like topologies [15] and [16], utilizes 1 additional power switch compared to [17] and [18]. However, as illustrated in Fig. 6 and Table 2, the proposed topology significantly reduces voltage stress across components and minimizes inductor current ripple compared to [15] – [18] topologies. Although the proposed topology involves a higher component count than [15] – [18], the overall cost remains comparable. Additionally, the total harmonic distortion (THD) of the proposed inverter and topologies [15] – [17] is lower than that of topology [18], as [18] operates with only two harmonic orders at the output. The proposed topology uses more components than topology [18]. However, the voltages across the components are less than half of those in topology [18]. Furthermore, for applications requiring high-quality output voltage, the proposed topology results in lower THD due to its operation as a three-level inverter, as opposed to a two-level inverter like [18]. The use of more components is a trade-off worth considering when evaluating the benefits in terms of THD, voltage stress on the components, and the inverter's output power.

4. Simulation and experimental results

4.1. Simulation results

To verify the DPWM method's efficacy with the suggested 3L-AqZS-T^{2}I configuration, simulations were performed using PSIM software. The parameters set for the simulation are displayed in Table 3.

The 3L-AqZS-T^{2}I topology is supplied with an input voltage of 200V. With a modulation index M is 0.885, a duty cycle d_0 is 0.5 and short-circuit ratio d is 0.115, the output voltage across the load is 110 V_{rms}.

Table 3: Simulation Parameters

Parameter/ Components		Values
Input voltage	V_{dc}	200 V
Output voltage	V_{RMS}	110 V_{RMS}
Output frequency	f_0	50 Hz
Switching frequency	f_s	10 kHz
Boost capacitors	C_{1P}, C_{2P}, C_{1N}, C_{2N}	1 mF
Boost inductors	L_{1P}, L_{2P}, L_{1N}, L_{2N}	500 uH
LC filter	L_f , C_f	3 mH and 10 µF
R-load	R_X	40-Ω

With a duty ratio d_0 = 0.5 and an input voltage V_{dc} = 200V, the semiconductor switches in the AqZS are controlled to generate an inverter input voltage V_{PN} with a peak value of 305V, the voltages across the capacitors are V_{C1P} = 35.12V and V_{C2P} = 17.56V, as shown in Figures 7(a) and 7(c).

To the symmetric nature of the 3L-AqZS-T^{2}I topology, the current through the inductor and the voltage across the capacitor on the upper side of the AqZS will be used for analysis. Figure 7(b) presents the waveform of the inductors current on the upper side of the AqZS I_{L1P}, I_{L2P}.

The pole voltage in phase A V_{AO} has three levels: $+V_{PN/2}$, 0, $-V_{PN/2}$. The output load currents waveforms are sinusoidal, with RMS values of 2.75A, as shown in Figure 8(b). The input current on the inverter side has an average value of 4.6A, as presented in Figure 8(c). However, the peak input current on the inverter side reaches up to 17.6A.

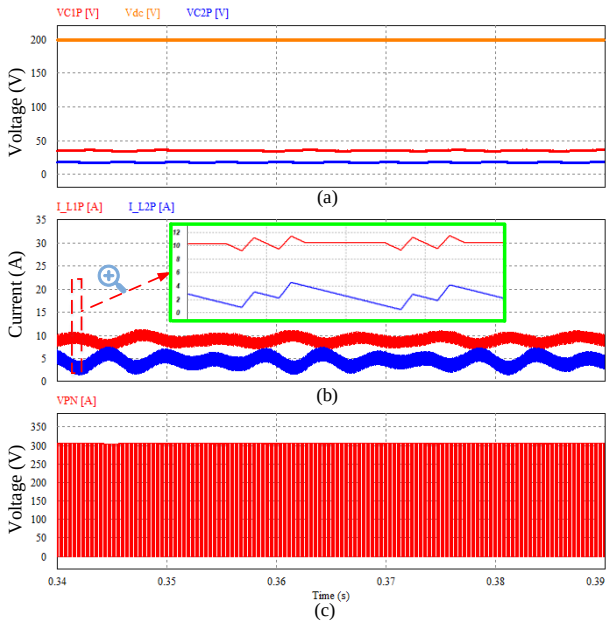

Figure 7: (a) The voltage across the capacitor V_{C1P} and V_{C2P}, (b) The current through upper inductors of AqZS ,(c) The DC-link voltage V_{PN}.

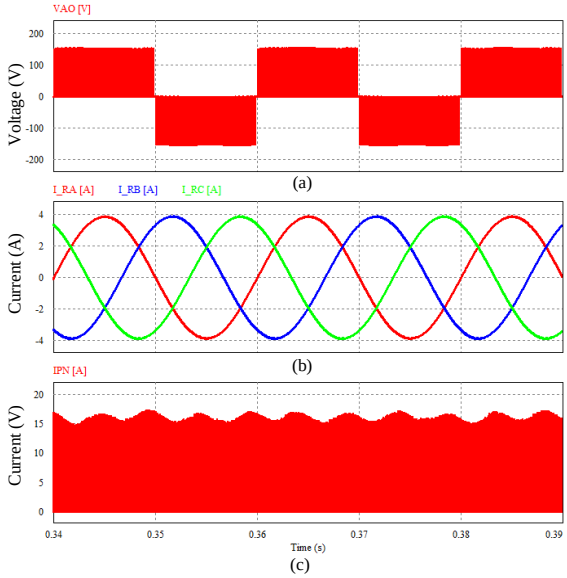

Figure 8: (a) The pole voltage V_{AO}, (b) The load current I_{RA}, I_{RB}, I_{RC} , (c) The input current I_{PN}.

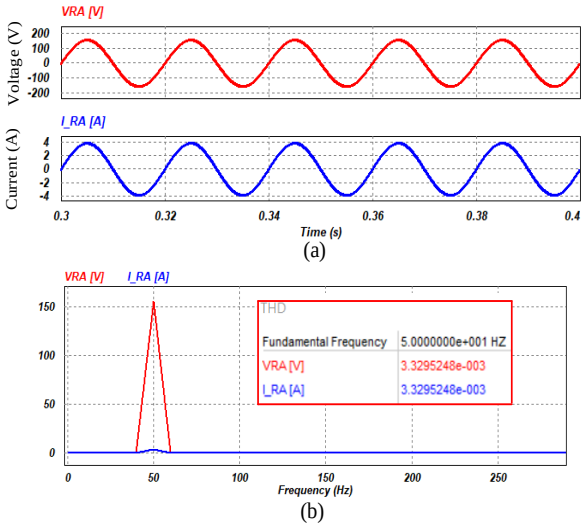

Figure 9: (a) Load current and voltage at phase A, (b) FFT analysis of load voltage and current at phase A.

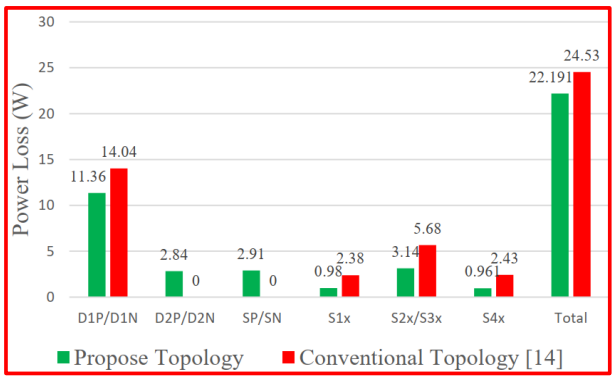

Figure 10: Calculation results compare power loss between proposed topology and conventional topology.

The load current and voltage in phase A are presented in Figure 9a), with the voltage and current values being 109.8 V_{RMS} and 2.75 A, respectively. Figure 9(b) shows the harmonic components at the fundamental frequency of the current and voltage in phase A. The THD of the current and voltage at the fundamental frequency is 0.33%.

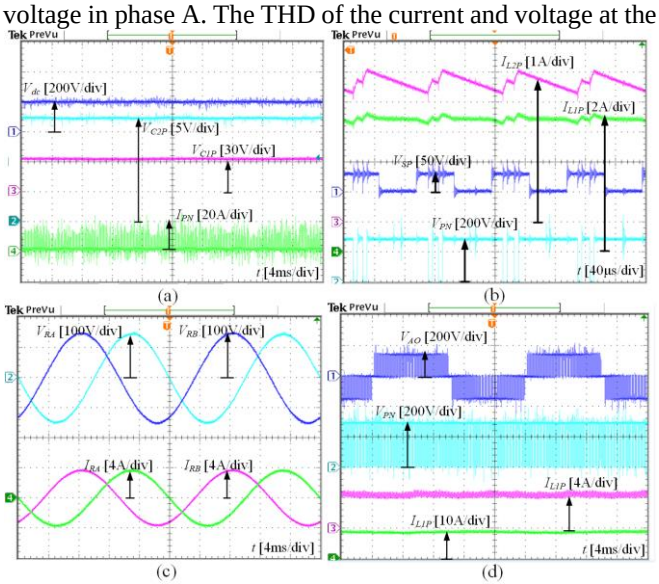

Figure 11: Experimental results for 200V input voltage.

By evaluating the power loss components in the device, as shown in [13], it can be observed that the proposed configuration has approximately 10% lower power loss compared to the traditional configuration [14]. Figure 10 illustrates the calculation results when the configurations operate at a power level of 0.5 kW.

4.2. Experimental Results

The proposed inverter's functionality has been verified through the development of a lab prototype that makes use of the DSP TMS320F28335. Twelve IGBT modules are used in the inverter side circuit (SKMGD123D). The MOSFETs 60R060P7, the diode VS-60APF12-M3, 1mF capacitors, and 500uH inductors are used to build the impedance source network. A 40 Ω three-phase resistive load is attached and fed through an LC filter (3 mH and 10 μF) to lower the output voltage's high-frequency components in order to test the suggested inverter. Table 2 lists all of the system parameters in detail.

Initially, the inverter was tested in boost mode using an input source of 200 V. Figure 11 displays the experimental findings

for the 200 V input voltage. The AqZS is utilized to boost the DC-link voltage, V_{PN}. In this test, parameters of d, d_0, M are set to be similar in simulation results. With these parameters, the capacitors voltages V_{C1P} and V_{C2P} on the upper side of AqZS, are boosted to 34.2 V and 16.9 V, respectively, as shown in Figure 11(a).

As a result, the voltage stress on the S_P switch is 34.9 V, the peak of V_{PN} voltage is 302 V, and Figure 11(b) shows the zoomed-in waveforms of the two inductor currents, I_{L1P} and I_{L2P}. Because an LC filter is being used, the output load voltage and current waveforms are sinusoidal, as seen in Figure 11(c), with RMS values of 104 V_{RMS} and 2.6 A_{RMS}, respectively. The inductor currents, I_{L1P} and I_{L2P}, are continuous with average values of 4.47 A and 8.89 A, respectively, although the input current is discontinuous with an average value of 4.43 A. As seen in Figure 11(d), the pole voltage in phase A V_{AO} has three levels: $+V_{PN}/2$, 0, and $-V_{PN}/2$.

5. Conclusion

The 3L-AqZS-T^{2}I topology can be applied in industrial systems with low to medium power ranges, utilizing the DPWM control method. The achieved output voltage and current results meet the required technical specifications. Both experimental and simulation results demonstrate that the voltage stress on the components of the proposed topology is lower than that observed in previous studies. The use of the ST state insertion algorithm and DPWM scheme enhances output voltage efficiency while minimizing the number of switching events in the system. To support the proposed method, the study includes detailed circuit analysis and operational theory. The accuracy of the proposed method has been validated through PSIM simulation software, as the simulation results are consistent with the calculations. Overall, the 3L-AqZS-T^{2}I topology performs well and holds potential for practical applications in industrial systems, including grid-connected PV systems, telecommunications, and uninterruptible power supply (UPS) units.

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