Investigate model and reduction technique of common-mode noise for LLC resonant converter

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Abstract

Switch Mode Power Supplies (SMPS) are extensively employed in fields such as telecommunications, information technology, and electric vehicles, where energy efficiency is increasingly demanded. Modern SMPS designs prioritize compact size, high power density, and optimal efficiency to meet these requirements. The LLC resonant topology, commonly utilized in the DC/DC conversion stage with planar transformers, enables operation at high frequencies (hundreds of kHz) and facilitates soft switching across the full load range. However, a significant drawback of this topology is electromagnetic interference (EMI), particularly common-mode (CM) noise, which arises from high switching frequencies and parasitic capacitance in the components. This challenge is further exacerbated by the use of planar transformers. This study presents a CM noise model for the Half-Bridge LLC (HB-LLC) converter based on a two-capacitor transformer representation, aiming to analyze CM noise behavior and investigate practical, cost-effective methods for its reduction.

Keywords: *Common-mode (CM) noise, half-bridge (HB) LLC resonant converter, electromagnetic interference (EMI), Inter-winding capacitance (IWC)*

1. Introduction

SMPS are extensively used in various fields, particularly in telecommunications, information and communication technology, and electric vehicles. Figure 1 illustrates the typical topology of an SMPS. The AC/DC stage is responsible for converting alternating current (AC) to direct current (DC), with power factor correction (PFC) techniques often employed to enhance efficiency and ensure stable, safe output power. This not only protects connected devices and users but also helps maintain the stability of the electrical grid. The subsequent DC/DC stage further processes the intermediate DC voltage, converting it into the desired output DC voltage to meet specific application requirements.

With the increasing demand for energy-efficient solutions, the design and development of SMPS are increasingly centered on achieving compact size, high power density, and superior efficiency. LLC resonant converters have become a preferred choice for DC/DC stages due to their ability to achieve soft switching, which significantly reduces switching losses [1]. This capability allows LLC converters to operate at switching frequencies in the hundreds of kilohertz, reducing the size of magnetic components and improving overall power density. Furthermore, planar transformers are increasingly replacing traditional wound transformers, offering advantages such as a low profile, enhanced efficiency, and improved thermal management [2]. However, the integration of LLC resonant converters with planar transformers presents challenges related to EMI, particularly conducted emissions.

Conducted emissions SMPS consist of two primary components: common-mode (CM) noise and differential-mode (DM) noise. Figure 2 illustrates the propagation paths of both CM and DM noise within an SMPS. DM noise arises from currents flowing in opposite directions along the power lines (depicted as blue noise currents), while CM noise consists of currents flowing in the same direction through the power lines, coupling via parasitic capacitance and returning through the protective earth (PE) (depicted as red noise currents). To measure EMI, a Line Impedance Stabilization Network (LISN) is typically employed, which detects noise through its internal resistor [3]. A bulk DC capacitor is strategically placed between the AC/DC and DC/DC stages to provide hold-up time and mitigate oscillations at twice the high DC voltage frequency. This capacitor, in conjunction with the large PFC inductor, significantly attenuates DM noise generated by the DC/DC stage before it reaches the LISN [4]. Consequently, CM noise becomes the dominant contributor to total EMI emissions in LLC resonant converters, necessitating a comprehensive investigation. This CM noise is mainly caused by parasitic capacitance and voltage change

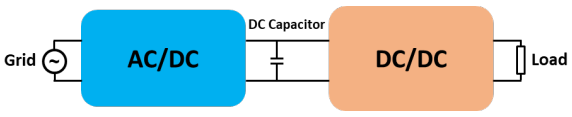

Figure 1: The typical topology of SMPS

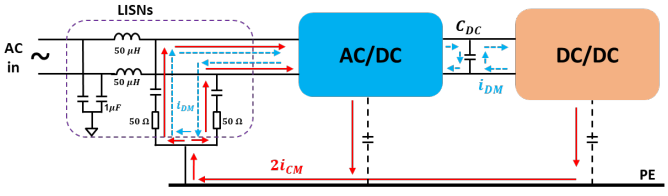

Figure 2: CM and DM noise paths in SMPS

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rate (dv/dt) [5]. Operating at high frequencies inherently involves rapid switching of semiconductor devices, resulting in a high dv/dt, which significantly contributes to elevated levels of CM noise. Additionally, compared to conventional wire-wound transformers, planar transformers exhibit substantially larger interwinding capacitances (IWC)—the parasitic capacitance between the primary and secondary windings. This increased capacitance provides a dominant pathway for CM noise currents to propagate from the primary side to the secondary side of the converter [6], [7]. Excessive CM noise can lead to non-compliance with electromagnetic compatibility (EMC) standards such as CISPR22 and EN55022. Details of standard and measurement methods are presented in detail in [8].

Effective CM noise mitigation strategies are essential to ensure regulatory compliance and reliable operation. EMI filters are commonly employed to ensure converters comply with EMC standards. However, these filters typically occupy one-third to one-fourth of the converter's total volume [9], significantly reducing overall power density. To address this limitation, shielding techniques for planar transformers are increasingly utilized, as they effectively mitigate CM noise without compromising power density [10], [11]. This approach involves placing shielding layers between the primary and secondary windings to block CM noise propagation through the transformer. While effective, integrating shielding layers into the PCB considerably increases manufacturing costs. In summary, although these CM noise reduction methods are effective, they are constrained by trade-offs, including higher production costs or reduced compactness.

This paper presents a formulation of the CM noise model for the LLC converter aimed at evaluating the impact of parasitic capacitance and noise sources, as introduced in [12]. Based on this model, this paper investigates several simple and cost-effective CM noise reduction techniques, as referenced in [13] and [14]. In [13], the implementation of a common-mode capacitor C_z is proposed to establish a low-impedance path for CM noise currents. However, C_z only effectively mitigates high-frequency noise. In [14], a compensation winding and a compensation capacitor are utilized to generate an anti-noise current that counters the CM noise current. Nevertheless, this technique proves to be effective primarily in the low-frequency range. To overcome the limitations of these individual methods, a combined approach integrated both techniques is proposed to enhance CM noise suppression across a wider frequency spectrum. Simulation and experimental results for a 300W, 250 kHz, 380V/60V HB-LLC converter are provided, demonstrating the accuracy of the proposed model and validating the effectiveness of the noise reduction methods.

2. Half-bridge LLC Resonant Converter CM Noise Model

An electrical circuit can be modeled as having parasitic capacitances connected to the PE from each node within the circuit. However, attempting to calculate and model all these parasitic capacitances can be cumbersome and complex. Therefore, the CM noise model focuses on a limited number of regions within the circuit that have a significant impact. In the case of the HB-LLC converter, the relevant parasitic capacitances are illustrated in Fig. 3. The CM noise current path is represented by the dashed lines, which include the interwinding capacitance C_{ps} between the primary and secondary windings, the parasitic capacitance C_Q between the midpoint of the half-bridge and PE, and the capacitances C_{1N} and C_{2N} between the diode terminals and PE. Additionally, a parasitic capacitance transformer model is developed to enable further calculation and modeling of the CM noise.

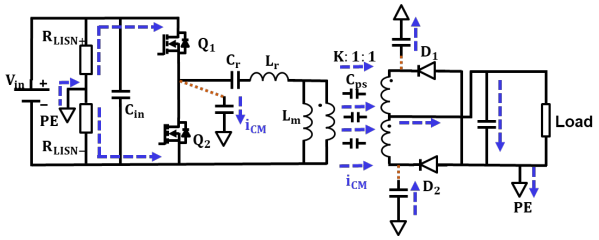

Figure 3: CM noise propagation in HB-LLC converter

Several transformer parasitic capacitance models have been proposed in prior research [4, 10, 15, 16]. In [16], these models are applied to analyze both DM and CM noise in power converters. To simplify CM noise analysis, [15] introduces an equivalent lumped capacitance model, ensuring the displacement current matches that of the actual transformer. The CM noise models in [4] and [10] are derived under the assumption that the transformer's leakage inductance serves as the resonant inductor.

This paper adopts the two-capacitor transformer model for the HB-LLC converter configuration, which features an external resonant inductor, minimal leakage inductance, and a primary side connected to an independent voltage source [12]. The equivalent lumped capacitance model of the transformer is depicted in Fig. 4(a). Based on the parasitic capacitance model, the CM noise model for the HB-LLC converter is formulated by referencing [12], [6] and [13].

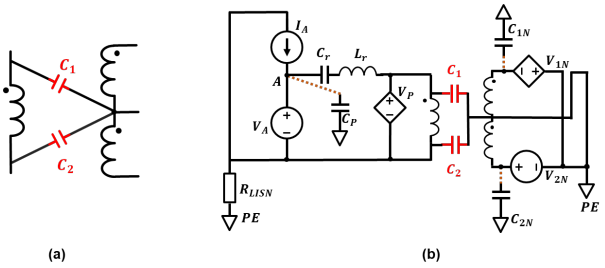

Figure 4: (a) Two-capacitor model of transformer (b) HB-LLC CM noise model with substituted source

To derive the CM noise model, the power switches in Fig. 3 are replaced with equivalent voltage and current sources using substitution theory. Specifically, on the primary side, the power switches Q_1 and Q_2 are replaced by a voltage source V_A and a current source I_A. On the secondary side, the diodes D_1 and D_2 are substituted with voltage sources V_{1N} and V_{2N}, respectively. The resulting simplified CM noise model is shown in Fig. 4(b). The CM noise generated by the voltage and current sources is analyzed based on superposition theory, as introduced in [13]. Based on [13], only v_P contributes to the generation of CM noise. Finally, the final CM noise model for the HB-LLC converter is illustrated in Fig. 5. Using equivalent circuit transformations, the CM noise current i_{CM} is determined by (1). The equivalent capacitance C_{eq}, representing C_1 and C_2, is

calculated using (2), while the equivalent noise source V_{eq} is derived using (3).

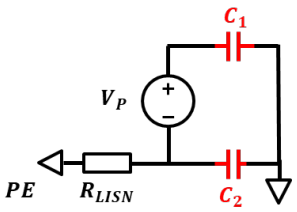

Figure 5: Final CM noise model

$$i_{CM} = C_{eq} \cdot \frac{dV_{eq}}{dt} \tag{1}$$

$$C_{eq} = C_1 + C_2 \tag{2}$$

$$V_{eq} = V_P \cdot \frac{C_1}{C_1 + C_2} \tag{3}$$

For the LLC converter, during the dead time, the slew rate of V_P can be approximated by V_A, and its voltage change rate is assumed constant, considering the capacitors being charged and discharged as linear capacitors [13]. The voltage waveforms of V_P and the noise current i_{CM} are shown in Fig. 6. The equivalent noise source and the amplitude of the CM noise current are recalculated in (4) and (5), respectively. Using the Fast Fourier Transform (FFT) as described in [11], i_{CM} is analyzed in (6). The CM noise voltage detected by the LISN is subsequently calculated in (7).

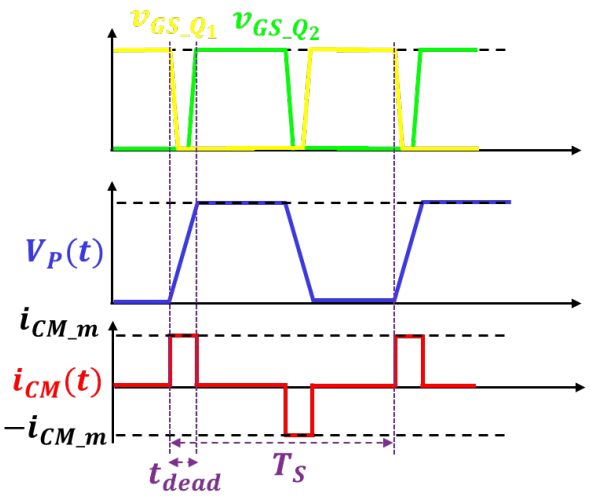

Figure 6: Voltage applied to the transformer's primary winding and the resulting common-mode current

$$V_{eq} = V_A \cdot \frac{C_1}{C_1 + C_2} \tag{4}$$

$$I_{CM\_m} = C_1 \cdot \frac{V_A}{t_{dead}} \tag{5}$$

$$i_{CM}(t) = I_{CM\_m} \frac{4t_{dead}}{T_S} \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(n\pi \frac{t_{dead}}{T_S}\right)}{n\pi \frac{t_{dead}}{T_S}} \sin\left(\frac{2n\pi}{T_S} t\right) \tag{6}$$

$$v_{CM}(t) = I_{CM\_m} \cdot R_{LISN} \frac{4t_{dead}}{T_S} \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(n\pi \frac{t_{dead}}{T_S}\right)}{n\pi \frac{t_{dead}}{T_S}} \sin\left(\frac{2n\pi}{T_S} t\right) \tag{7}$$

where t_{dead} is the dead time and T_S is the duty cycle of the HB-LLC converter.

Table 1: Specifications of the HB-LLC converter

Components	Value
Power	300 W
Input voltage	380 V
Output voltage	60 V
Magnetizing inductance (L_m)	142 μH
Resonant inductance (L_r)	20.4 μH
Resonant capacitance (C_r)	19.8 nF
Resonant frequency (f_r)	250 kHz
Lump capacitance (C_1)	435 pF
Lump capacitance (C_2)	435 pF
Dead time (t_{dead})	213 ns

To validate the accuracy of the CM noise model for the LLC resonant converter, simulations using LTspice XVII and experimental measurements were conducted on a 380V/60V HB-LLC converter. The parameters of the LLC converter are listed in Table 1. The capacitance values C_1 and C_2 were determined via measurements, as described in [12]. The measurement setup is illustrated in Fig. 7.

In Fig. 7(a), the total primary-to-secondary capacitance, C_{IWC}, was measured using an LCR meter. In Fig. 7(b), the voltages v_1 (between terminals A and D) and v_2 (between terminals B and D) were recorded using an oscilloscope. The capacitance values C_1 and C_2 were then calculated using (8). The results are presented in Fig. 8.

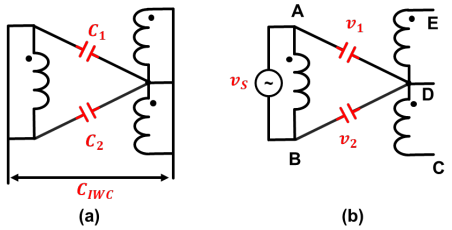

Figure 7: (a) Measure total primary to secondary capacitance C_{IWC} , (b) Measure voltage v_{AD} và v_{BD}.

$$\begin{cases} C_1 = C_{IWC} \frac{v_2}{v_S} \\ C_2 = C_{IWC} \frac{v_1}{v_S} \end{cases} \tag{8}$$

The experimental setup is illustrated in Fig. 9. The CM noise spectrum, calculated using (7), is compared with simulation and experimental results in Fig. 10, covering the frequency range of 150 kHz to 30 MHz. As shown in Fig. 10, the experimental, simulated, and calculated noise voltages align closely within the frequency range of 150 kHz to 4 MHz. However, deviations are observed beyond 4 MHz. These discrepancies arise due to the nonlinear behavior of the charging and discharging

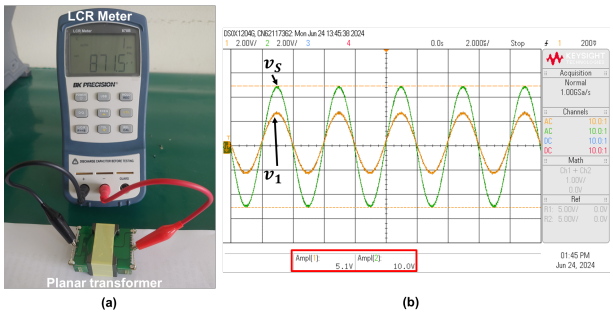

Figure 8: Measurement results (a) C_{IWC}, (b) v_1 and v_S

capacitances of the power switches, which were assumed to be linear in the analytical model. Furthermore, the approximation of the voltage change rate V_P by V_A and the short-circuiting of input and output capacitors in the model contribute to the observed differences. In summary, the model exhibits high accuracy at lower frequencies, while deviations become apparent at higher frequencies.

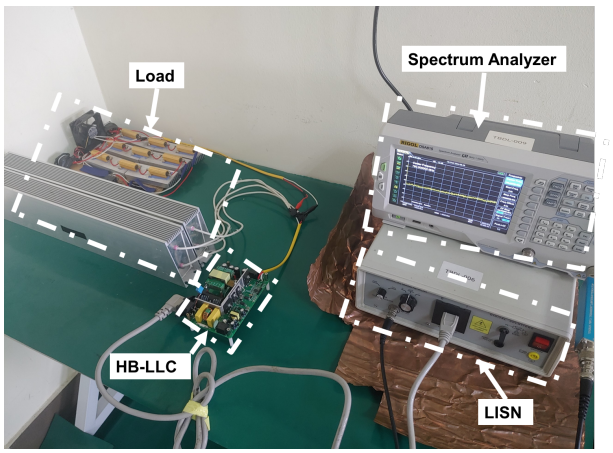

Figure 9: Experiment setup

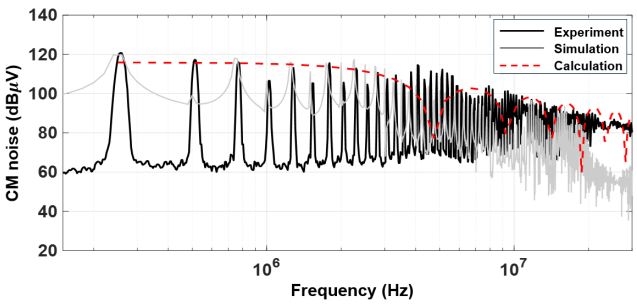

Figure 10: Results of verifying the noise model

3. Common-mode Noise Reduction Approaches for LLC Converter

As discussed above, the primary sources of CM noise are parasitic capacitance and dv/dt. Therefore, it is essential to address these factors in order to mitigate CM noise. This section presents methods for disrupting the noise path and eliminating the noise source.

3.1. Common-Mode Capacitance Approach

The operating principle of the common-mode capacitor C_z is similar to that of the Y capacitor in an EMI filter. Typically, C_z is connected between the primary side and the secondary side of the transformer, which is grounded through the PE, as shown in Fig. 11. Its primary function is to provide a low-impedance path for CM noise currents. As a result, the CM noise current flows through C_z and returns to the primary side, rather than flowing to the PE, thus effectively reducing the CM noise current. This phenomenon can be illustrated through the CM noise model shown in Fig. 12.

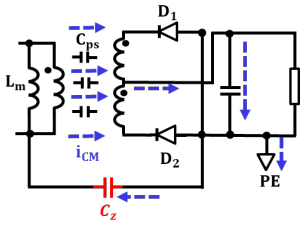

Figure 11: Common-mode capacitor in HB-LLC converter

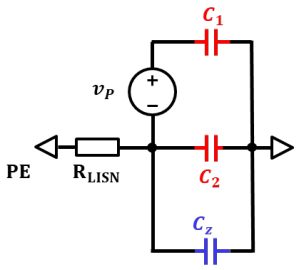

Figure 12: CM noise model with common-mode capacitor

Based on the CM noise model with the common-mode capacitance C_z, the CM noise current is calculated using the following formula:

$$\dot{I_{CM}} = \frac{\dot{V_P}}{Z_{C_1} + (\frac{R_{LISN}}{Z_{C_t}})} \tag{9}$$

where C_t is the sum of C_1, C_2, and C_z, Z_{C_1}, Z_{C_t} are impedance of C_1, C_t.

From (9), it follows that increasing the capacitance C_z reduces the CM noise current. However, in isolated DC/DC converters, the presence of capacitor C_z also contributes to an increase in leakage current from the primary to the secondary side [17]. Therefore, the value of C_z must be carefully constrained to ensure user safety. In practice, the leakage current is typically limited to 3.5 mA.

Fig. 13 illustrates the CM noise levels before and after the addition of an 11.1 nF capacitor C_z. Experimental results indicate that C_z effectively mitigates high-frequency noise, achieving a reduction of 10–15 dBμV. In conclusion, the common-mode capacitor noise reduction method is straightforward and simple to implement. Although it is limited by the capacitor value, which results in a modest reduction in CM noise, the capacitor C_z can still significantly reduce the size and cost of the EMI filter.

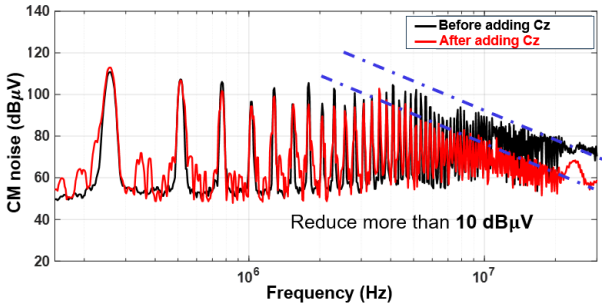

Figure 13: Experimental results of CM noise before and after adding Cz

3.2. Passive noise compensation approach

The idea of the passive noise compensation method is to generate a current that is balanced and opposite to the noise current flowing into the PE, thereby significantly reducing the CM noise [14].

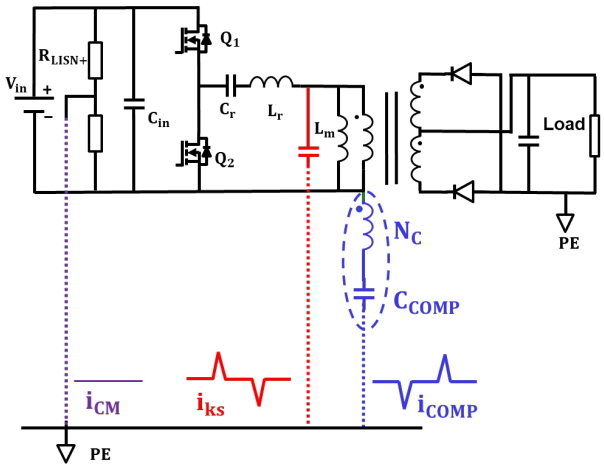

Figure 14: The LLC resonant converter using passive noise compensation

Fig. 14 illustrates the structure of the HB-LLC converter with passive noise compensation. The red current represents the CM noise current generated by the converter, while the supplementary circuit introduces the blue anti-noise current. In an ideal scenario, the sum of these two currents cancels out, thereby reducing CM noise. This is achieved by using the compensation winding N_C to generate a 180° out-of-phase waveform across the compensation capacitor, resulting in the anti-noise current i_{COMP}. Since N_C only carries the anti-noise current i_{COMP}, it can be wound with much smaller wire compared to the primary and secondary windings. The CM noise model incorporating passive noise compensation is shown in Fig. 15, where v_{COMP} represents the voltage source generated by N_C, and C_{COMP} is the noise compensation capacitor. Based on this CM noise model, the CM noise current can be calculated using the following formula:

$$\dot{I_{CM}} = \frac{(\frac{\dot{V_P}}{Z_{C_1}} - \frac{\dot{V_{COMP}}}{Z_{C_{COMP}}}) \cdot Z_{C_{td}}}{Z_{C_{td}} + R_{LISN}} \tag{10}$$

Thus, to cancel the CM noise current, $\dot{V_{td}}$ must be equal to 0.

This mean:

$$\frac{\dot{V_P}}{Z_{C_1}} = \frac{\dot{V_{COMP}}}{Z_{C_{COMP}}} \tag{11}$$

or

$$\dot{V_P} \cdot C_1 = \dot{V_{COMP}} \cdot C_{COMP} \tag{12}$$

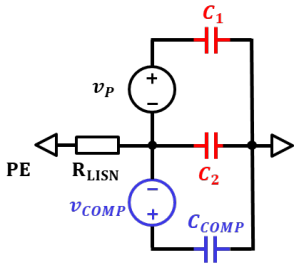

Figure 15: CM noise model using passive noise compensation

The number of turns of the winding N_C and the value of the capacitor C_{COMP} are selected to satisfy the condition in (12). Therefore, as the number of turns of the winding N_C increases, the required value of the capacitor C_{COMP} decreases, and vice versa. However, increasing the number of turns also raises the leakage inductance and parasitic capacitance of the winding, which may lead to high-frequency noise due to resonance between the compensation capacitor and the leakage inductance [14].

Fig. 16 illustrates the CM noise levels before and after the addition of a 2-turn compensation coil N_C and a 4.5 nF compensation capacitor C_{COMP}. Experimental results show that the compensation approach is effective in reducing low-frequency noise, achieving a 10 - 15 dBμV reduction. However, the reduction becomes less effective at higher frequencies due to resonant phenomena and the bandwidth limitations of the transformer [18].

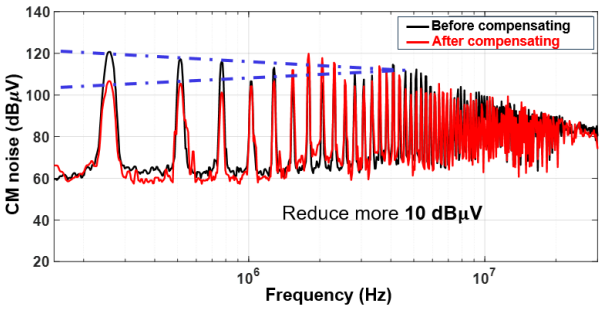

Figure 16: Experimental results of CM noise before and after using noise compensation method

In short, similar to the common-mode capacitor approach, the passive noise compensation method is simple, easy to implement, low-cost, and effective. However, its application should be approached with caution. Passive noise compensation is only effective when the compensation winding and primary inductor are well-coupled, and the compensation capacitor is accurately chosen to satisfy (12). Therefore, precise calculation of parasitic capacitors, compensation capacitors, and transformer design is essential for the method's effectiveness.

3.3. Combining the passive noise compensation approach and the common-mode capacitor approach

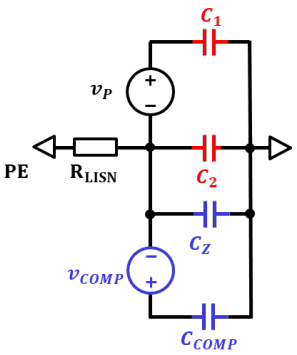

Figure 17: CM noise model using combination approach

Since the common-mode capacitor method is effective in mitigating high-frequency noise, while the passive noise compensation method excels in reducing low-frequency noise, a combination of both methods can be employed to reduce common-mode noise across the entire frequency spectrum. The CM noise model of this combination approach is shown in Fig. 18. Base on this model, the CM noise current can be calculated using the following formula:

$$\dot{I_{CM}} = \frac{(\frac{\dot{V_P}}{Z_{C_1}} - \frac{\dot{V_{COMP}}}{Z_{C_{COMP}}})}{1 + \frac{R_{LISN}}{Z_{C_{td}}}} \tag{13}$$

where C_{td} is the sum of C_1, C_2, C_z and C_{COMP}, $Z_{C_{td}}$ are impedance of C_{td}.

Similar to section 3.2, the numerator of (13) equal to zero. However, in practice, it cannot be exactly zero due to the presence of resonance phenomena. Hence, the addition of capacitors C_Z also contributes to reducing I_{CM}.

The comparison of CM noise voltage among the combination approach, the common-mode capacitance approach and the passive noise compensation approach is presented in Fig. 18. The results demonstrate that the simultaneous application of both noise reduction techniques achieves superior effectiveness compared to the individual implementation of each method. In particular, the CM noise voltage is decreased 10 dBµV to over 15 dBµV across the frequency range. However, as presented in section 3.2, the resonance phenomenon and the bandwidth limitations of the transformer continue to affect the effectiveness of noise reduction. Indeed, in Fig. 18, the CM noise voltage is not reduced at 4 MHz.

In conclusion, this section has examined two methods for reducing CM noise that are straightforward to implement, cost-effective, and compact in size. The common-mode capacitor approach is particularly effective in the high-frequency range, whereas the passive noise compensation method targets the low-frequency range. When combined, these methods provide comprehensive noise reduction across the entire frequency spectrum. The choice of method should be based on the specific requirements of the application.

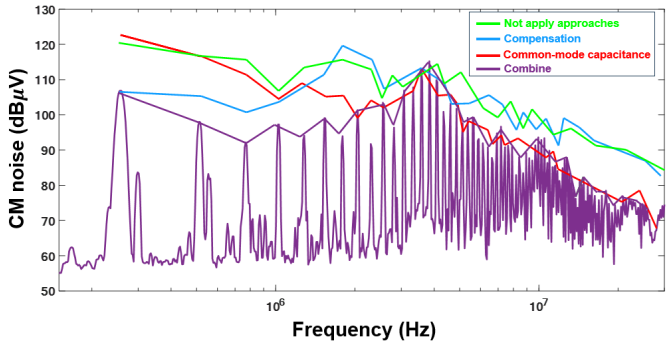

Figure 18: Experimental results of CM noise voltage among the combined approach, the common-mode capacitance approach, and the passive noise compensation approach

4. Conclusion

This paper investigates CM noise in LLC resonant DC/DC converters with external resonant inductors. A CM noise model is proposed, based on a two-capacitor transformer approach. The model's accuracy is validated through both simulation and experimental results on a 300W, 380V/60V HB-LLC converter. Furthermore, this study explores simple and effective techniques for CM noise mitigation. The common-mode capacitance approach effectively reduces CM noise voltage by more than 10 dBµV in the high-frequency range, while the passive noise compensation technique achieves an attenuation of 10–15 dBµV in the low-frequency range. Moreover, the combined implementation of both approaches provides a comprehensive solution, ensuring effective CM noise suppression across the entire frequency spectrum. However, the integration of two noise reduction approaches does not mitigate the inherent limitations associated with individual methods, such as the resonance phenomenon and the bandwidth constraints of the transformer.

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