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Single phase five-level quasi-switch boost inverter with high voltage gain

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Abstract

In this paper, a new topology incorporating the quasi-switch boost network and the five-level cascade H-bridge inverter has been presented. By using one more inductor and one more capacitor compared to conventional quasi-switch boost network, the voltage gain, as well as the voltage stress on power devices of an intermediate network, is significantly improved. In addition, the quality of the output voltage waveform is also improved by using a five-level cascade H bridge topology. The PWM control strategy for this topology is based on the carrier phase shift technique which ensures that each module of cascade form behaves as a three-level quasi-switch boost inverter. As a result, the output voltage of the converter has five-level. The shoot-through signal is inserted in the time interval, in which the output voltage of the inverter is zero in value to not affect the output voltage waveform. The simulation and experiment results are conducted to verify the accuracy of the introduced topology.

Keywords: *Cascaded H-bridge inverter; Five-level inverter; PWM strategy; Quasi-switched boost inverter; Shoot-through*

Symbols

Symbols	Units	Description
V_{dc}	V	Input voltage
I_R	A	Output load current
m		Modulation index
V_o	V	Output voltage
V_{a0}	V	Pole voltage
D_0		Duty cycle

Abbreviations

MI	Multilevel inverter
NPC	Neutral point clamped
FC	Flying capacitor
ST	Short through
Zs	Z-source
NST	Non-short through
UPS	Uninterruptable power supply
qZs	Quasi-Z-source
qSB	Quasi-switch boost
PWM	Pulse with modulation
CHB	Cascade H bridge
5L-CHB	five-level CHB
THD	Total harmonic distortion

Tóm tắt

Trong bài báo này, một cấu hình mới kết hợp giữa mạng nguồn kháng tựa khóa chuyển mạch và cấu hình nghịch lưu năm bậc ghép tầng dạng cầu H được trình bày. Bằng cách sử dụng thêm một cuộn dây và một tụ điện so với mạng nguồn kháng tựa khóa chuyển mạch truyền thống, độ lợi điện áp cũng như điện áp đặt trên các linh kiện điện tử công suất được cải thiện một cách đáng kể. Ngoài ra, chất lượng dạng sóng điện áp ngõ ra cũng được cải thiện do sử dụng cấu hình năm bậc ghép tầng cầu H. Phương pháp điều khiển độ rộng xung (PWM) cho cấu hình này dựa trên kỹ thuật dịch pha sóng mang, điều này đảm bảo mỗi module cầu H hoạt động như một mạch nghịch lưu tăng áp tựa khóa chuyển mạch 3 bậc. Kết quả là ngõ ra của bộ nghịch lưu có năm bậc điện áp. Tín hiệu ngắn mạch được chèn vào khoảng thời gian mà điện áp ngõ ra của mạch nghịch lưu có giá trị bằng zero để không ảnh hưởng đến dạng sóng điện áp ngõ ra. Kết quả mô phỏng và thực nghiệm được xây dựng để kiểm chứng cấu hình được trình bày.

1. Introduction

Recently, multilevel inverters (MIs) has been widely used for industrial applications due to its advantages such as better output voltage quality, smaller low-pass filter size requirement, lower voltage stress on switching devices compared to two-level inverter [1]-[2]. There are three basic topologies of MIs which are neutral point clamped (NPC) inverter, cascade, or flying capacitor (FC) inverter. Each topology has both particular advantages and disadvantages, but the common drawback of these types is that they are not able to operate under the short through (ST) condition which is generated when all switches in any phase leg are turned on simultaneously. Besides that, traditional topologies behave as buck dc-ac power conversion which produces output voltage whose peak-peak value is smaller than DC-link voltage.

To overcome these limits, the inverter based on Z-source (Zs) topology was explored by Prof. F. Z. Peng in [3]. By using one more diode, two additional inductors, and two additional capacitors, this topology is known as a single-

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stage converter with buck-boost capability and ST immunity. This topology operates in two main modes: non-short through (NST) mode and ST mode. This ST state is used to boost the DC-link voltage in order to achieve the desire AC output voltage at the load. This topology can solve the ST phenomenon, which causes the short-circuit phenomenon in the conventional inverter, without using dead-time which causes output distortion. Because of the benefits of Zs topology, it is widely applied to industrial and civil applications like PV system [4], uninterruptable power supply (UPS) system [5], etc. The literature [6] discussed a single-phase five-level inverter based on the Zs network. This study presented a combination of Zs network and single-phase five-level T-type topology, so it has all advantages of Zs network and MI such as buck-boost capability and good output waveform quality. Besides the benefits of this type of impedance network, Zs network also has some drawbacks such as discontinuous input current because of using input diode which causes stress on the input power supply which is not suitable for PV applications. In addition, the high voltage stress on the power capacitor is a significant disadvantage of this topology.

The literature [7] proposed a novel type of impedance network called quasi-Z-source (qZs) to improve the limitations of the Zs network. In this topology, the input current is continuous and voltage stress on capacitors is reduced significantly. To inherit the outstanding advantages of MI, a combination of the qZs network with a single-phase five-level inverter was discussed in [8]. This study used two identical qZs networks in cascade form to produce five-level at the output terminal. Therefore, it improves the quality of output voltage, but it also leads to an increase in the number of passive components such as capacitors and inductors, so weight, size, and cost of the system are increased significantly. On the other hand, the qZs network is not flexible to control because the boost factor depends on the ST duty ratio of inverter leg which is limited by *(1-M)*, where *M* is the modulation index.

With one more active switch, the quasi-switch boost (qSB) network saves one inductor and one capacitor compared to the qZs topology whereas the boost factor is maintained [9]. In this study, the single-phase three-level H-bridge was considered to incorporate with the qSB network. However, the inductor current ripple of this structure is quite large. The literature [10] presented a pulse with modulation (PWM) scheme based on phase shift carrier method to reduce the inductor current ripple and enhance the boost factor of the converter. Two cascades H-Bridge (CHB) was incorporated with two qSB networks to produce a single-phase five-level qSB inverter which are proposed in [11]. However, the topology of the intermediate network and the PWM method used in [11] generates output voltage with low voltage gain and high voltage stress on devices. By using one more inductor and one more capacitor, the voltage gain and voltage stress on devices of the converter are significantly improved [12]. In this study, the single-phase HB is used to produce a three-level voltage at output load voltage. Therefore, the quality of the output voltage is not higher than [11].

In this paper, a combination of qSB network and five-level CHB (5L-CHB) is introduced. A modified phase-shift carrier control method is considered to control the introduced topology to obtain a high boost factor with low current ripple in input inductor compared with [11]. Good quality of output voltage waveform is achieved by using the proposed structure. The rest of this paper is divided into three parts. Section 2.1 shows the introduced topology with its PWM control strategy. Section 2.2 presents the simulation and experimental results to verify the accuracy of the presented theory. Section 3 shows the summary of this paper.

2. Main Content

2.1. 5L- qSB-CHB Topology

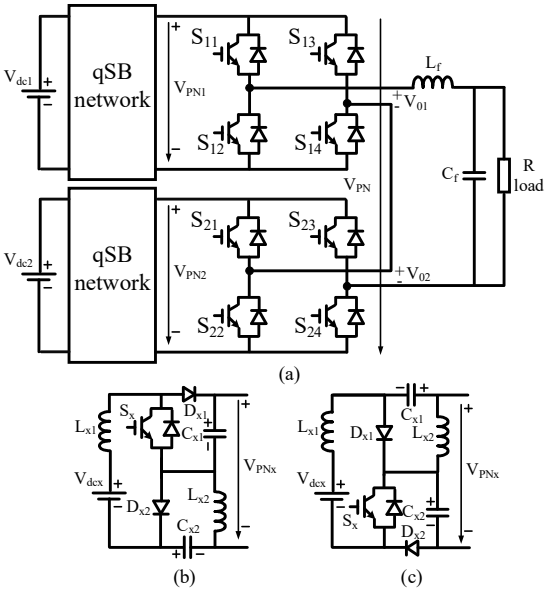


Figure 1. 5L-qSB-CHB. (x = 1, 2).

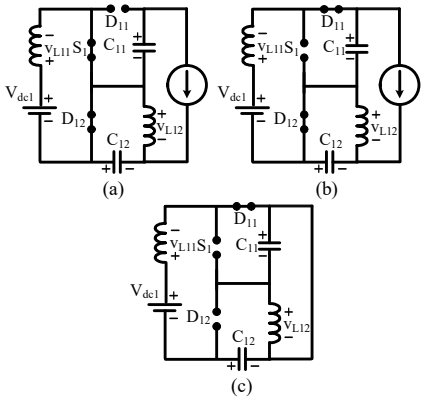


Figure 2. Operating states of the 5L-qSB-CHB. (a) NST mode 1 (b) NST mode 2, (c) ST mode.

Fig.1(a) illustrates the 5L-qSB-CHB topology. This structure consists of two identical modules which is three-level qSB-HB topology, each module is generated by placing an intermediate network (qSB network) before an H-Bridge circuit to boost the input power supply. There are two types of qSB network which is created by adding one inductor (L_{x2}, x=1, 2) and one capacitor (C_{x2}, x=1, 2) into a traditional qSB network presented in [9] which consist of one inductor (L_{x1}), one capacitor (C_{x1}), one active switch (S_x) and two diode (D_{x1} and D_{x2}), as shown in Fig. 1(b) and Fig.1(c). In general, these types of qSB networks have the same characteristic,

thus the configuration shown in Fig.1(b) is considered to analyze the operation of the converter. The H-Bridge is organized by four switches (S_{x1}, S_{x2}, S_{x3}, S_{x4}) which is able to generate a three-level voltage at the output which are $+V_{PNx}$, 0 and $-V_{PNx}$. The output of two modules is connected in series. Because these modules have the same structure, and the output of the introduced structure is the sum of the outputs of two modules, so there is the five-level voltage at the output of the proposed topology which are $+2V_{PNx}$, $+V_{PNx}$, 0 and $-V_{PNx}$, $-2V_{PNx}$. Because these modules have the same structure, module 1 is considered as an example to discuss the operating principle of the introduced topology.

Table 1. Switching states of 5L-qSB-CHB (x=1, 2).

Mode	Triggered Switches	ON Diodes	V_{OX}
NST 1	S_X, S_{X1}, S_{X4}	D_{X2}	$+V_{PN}$
	S_X, S_{X1}, S_{X3}		0
	S_X, S_{X2}, S_{X4}		0
	S_X, S_{X2}, S_{X3}		$-V_{PN}$
NST 2	S_{X1}, S_{X4}	D_{X1}, D_{X2}	$+V_{PN}$
	S_{X1}, S_{X3}		0
	S_{X2}, S_{X4}		0
	S_{X2}, S_{X3}		$-V_{PN}$
ST	S_{X1}, S_{X2}, S_{X3}, S_{X4}	D_{X1}	0

2.1.1. *Operation principles*

Similar to conventional qSB topology, this structure also operates under two main modes: NST mode and ST mode. In NST mode, the H-Bridge of each module is able to produce a three-level voltage at the output terminal by triggering corresponding switches in H-Bridge, as shown in Tab. 1. When S_{x1} and S_{x4} are switched "ON", the output voltage of the module achieves $+V_{PN}$ which is the DC-link voltage generated by the qSB network, while the output voltage obtains $-V_{PN}$ when S_{x2} and S_{x3} are turned "ON". The zero value is produced at output voltage when ether S_{x1} and S_{x3} or S_{x2} and S_{x4} are triggered "ON". The NST mode consists of two submodes which are NST1 and NST2, as presented in Fig. 2. The ST mode is achieved when all switches in inverter leg (H-Bridge) are triggered "ON". As a result, the output load voltage in this time interval is zero. Therefore, in order not to cause the distortion at output voltage waveform, the ST signal is inserted within the time interval which the output voltage is zero as shown in Fig. 3.

In NST 1 mode [see Fig. 2a], the switch S_1 is trigger "ON", so the diode D_{11} is reverse-biased, whereas, diode D_{12} is forward-biased. The inductor L_{11} stores energy from input power supply (V_{dc1}) whereas inductor L_{12} charges for the capacitor C_{12}. The energy of the intermediate network and input voltage source are transferred to the load through capacitor C_{11} and H-Bridge circuit. The voltage across two inductors are expressed as:

$$\begin{cases} V_{L11} = V_{dc1} \\ V_{L12} = V_{C12} \end{cases} \quad (1)$$

In NST 2 mode [see Fig. 2b], the switch S_1 is triggered "OFF", two diodes D_{11} and D_{12} are forward-biased. As a result, the capacitors C_{11} and C_{12} are charged from L_{11} and L_{12} respectively. The voltages of these inductors are calculated as:

$$\begin{cases} V_{L11} = V_{dc1} - V_{C11} \\ V_{L12} = V_{C12} \end{cases} \quad (2)$$

In ST mode, all switches of the H-Bridge circuit are turned "ON" simultaneously. As a result, the diode D_{12} is reverse-biased, whereas diode D_{11} is forward-biased. The inductor L_{11} is stored energy from capacitor C_{12} and an input voltage source, whereas the capacitor C_{11} charges for the inductor L_{12} through switches of the H-Bridge circuit. The voltages of two inductors are expressed as:

$$\begin{cases} V_{L11} = V_{dc1} + V_{C12} \\ V_{L12} = -V_{C11} \end{cases} \quad (3)$$

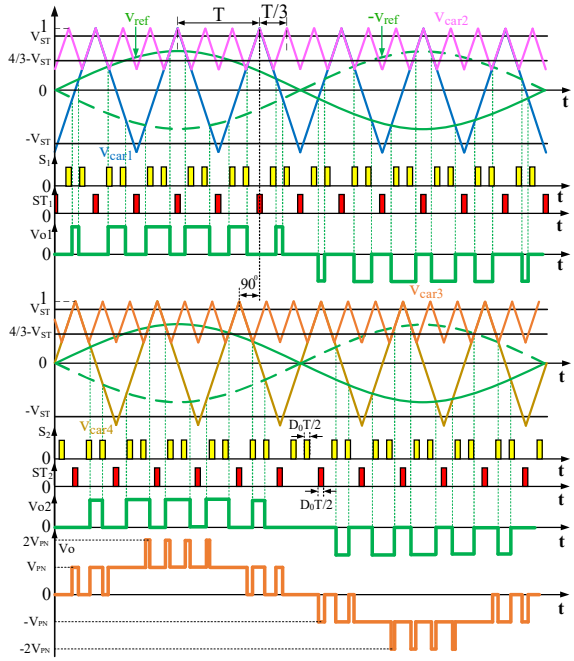


Figure 3. PWM strategy for 5L-qSB-CHB topology based on PS method.

2.1.2. *Steady-State Analysis for the Three-Level qSBT²I*

Fig. 3 illustrates the PWM strategy for the introduced topology. The control signal of switches S_1 and ST signal of H-Bridge circuit are identified by using two carriers V_{car1} and V_{car2} with three reference signals V_{ST}, $-V_{ST}$, and $(4/3\text{-}V_{ST})$. Similar to module 1, the ST signal of module 2 and control signal of switch S_2 are identified through V_{ST}, $-V_{ST}$, and $(4/3\text{-}V_{ST})$ and two carriers V_{car3} and V_{car4}, as shown in Fig. 3.

In each period cycle of carrier V_{car1}, the time interval for NST 1 is $2D_0T$, whereas the total time interval for ST mode is D_0T, where D_0 is the ST ratio of the H-Bridge circuit. The rest of the period cycle of V_{car1} is NST mode 2. Therefore, the time interval for this mode is $(T\text{-}3D_0T)$. Assume that the input source of two modules have the same value which is V_{dc}, by using the vol-second balance for two inductor L_{11} and L_{12} with the time interval for each mode which is identified above, the voltage across two capacitors of module 1 can be expressed as [12]:

$$\begin{cases} V_{C11} = \dfrac{1-D_0}{1-4D_0+2D_0^2} V_{dc} \\ V_{C12} = \dfrac{D_0}{1-4D_0+2D_0^2} V_{dc} \end{cases} \quad (4)$$

During operation, the peak value of the DC-link voltage of module 1 can be calculated by summing voltage across two capacitor C_{11} and C_{12}. Therefore, it can be calculated as [12]:

$$V_{DC-link} = V_{C11} + V_{C12} = \frac{1}{1-4D_0+2D_0^2} V_{dc} \quad (5)$$

So, the boost factor (B) can be identified as:

$$B = \frac{2V_{DC-link}}{V_{dc}} = \frac{2}{1-4D_0+2D_0^2} \quad (6)$$

In this way, the capacitor voltage and DC-link voltage of module 2 can be identified, similarly. The output of introduced topology is the sum of output of two modules, therefore, the peak value of output voltage is $+2V_{PN}$, as shown in Fig. 3. The peak-value of first-order harmonic of the output voltage is defined as:

$$V_{o,peak} = M \times B \times V_{dc} = \frac{2M}{1-4D_0+2D_0^2} V_{dc} \quad (7)$$

Where M is a modulation index. In order not to cause distortion on the output voltage, the relationship between M and D_0 must be:

$$\begin{cases} 0 \le M \le 1 \\ 0 \le M + D_0 \le 1 \end{cases} \quad (8)$$

The voltage gain (G) can be expressed as:

$$G = \frac{V_{o,peak}}{V_{dc}} = \frac{2M}{1-4D_0+2D_0^2} \quad (9)$$

2.1.3. *DC-link1 and DC-link2 Voltage Balance Control*

A simple DC-link voltage regulator based on the proportional-integral-derivative (PID) controller as shown in Fig. 4 is used to control the DC-link voltage of the introduced. Two DC-link 1 and DC-link2 voltages (V_{PN1} and V_{PN2}). V_{PN1} and V_{PN2} are fed back to determine the reference DC-link voltage (V_{PN}). The indirect feedback DC-link voltage is then compared with the reference value. The error of this comparator is entered to the PID controller to generate the duty cycle of the switch $S1$. The difference between V_{PN1} and V_{PN2} is minimized by the PID controller to generate the different duty ratio ΔD.

$$D_2 = D_1 + \Delta D \quad (10)$$

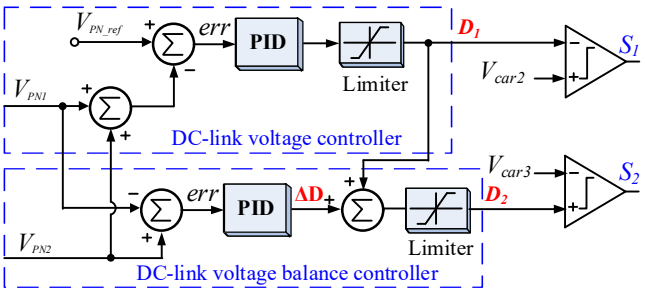


Figure 4. DC-link1 and DC-link2 Voltage Balance Control.

Based on equation (6) and (9), the boost factor (B) and the voltage gain (G) are investigated when the modulation index is set to (1-D_0). The results are compared to other configurations and PWM control methods presented in [6], [11]. As shown in Fig.5, the proposed structure and PWM control method provide superior boost factor and voltage gain compared to [6] and [11].

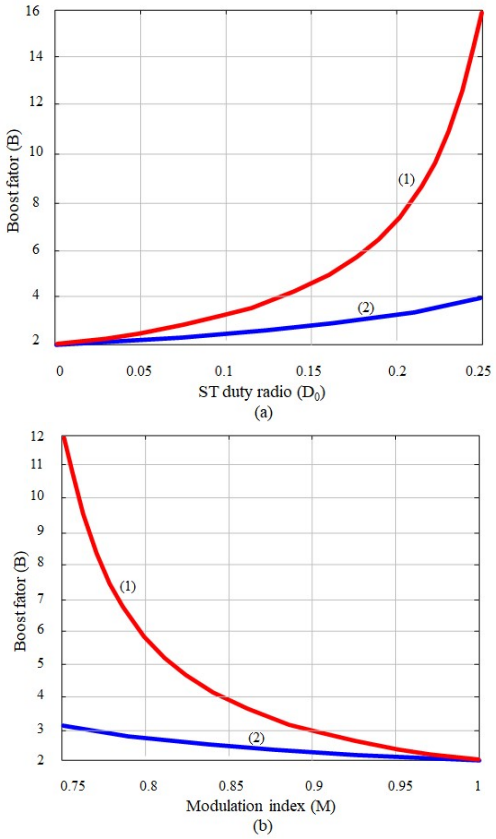


Figure 5. (a) Boost factor (B) vs ST duty ratio (D_0) and voltage gain (G) vs modulation index (M) of (1) proposed method, (2) the PWM method presented in [6],[11].

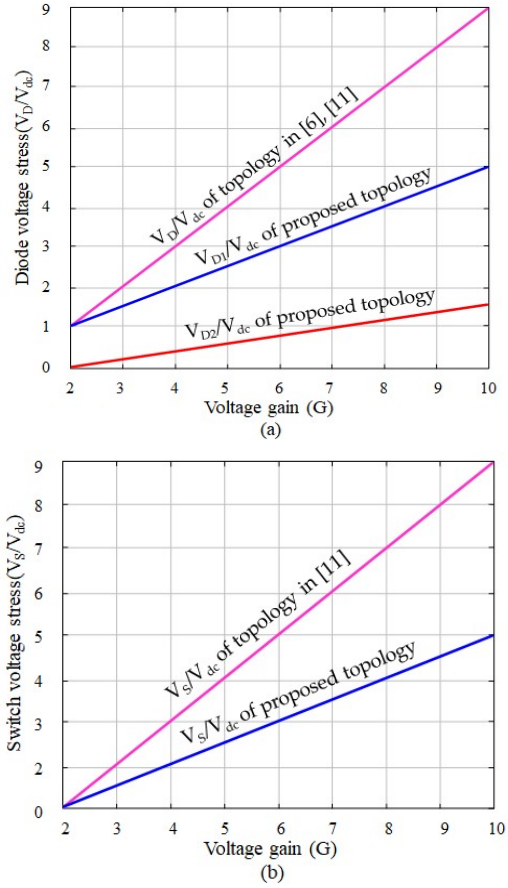


Figure 6. (a) Voltage gain (G) vs Diode voltage stress (V_D/V_{dc}) and voltage gain (G) vs Switch voltage stress (V_S/V_{dc}).

To demonstrate the superior of proposed method in voltage stress on power devices, two investigations are conducted which are the variation of diode voltage stress and switch voltage tress based on the variation of voltage gain. The results are presented in Fig. 6(a) and 6(b). It can be seen that when the voltage gain 5 the proposed topology with its PWM control method is produced less 62.5% the voltage stress on diode and switch of intermediate network compared to the topology presented in [6] and [11].

2.2. Simulation and Experimental Results

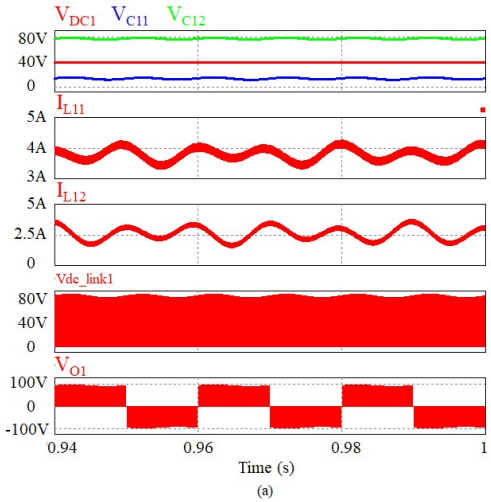
2.2.1. *Simulation results*

To demonstrate the effectiveness of introduced topology with the presented PWM control method, the simulation is constructed with the help of PSIM. The parameters used for simulation and experiment are presented in Tab.2. The input power supplies (V_{dc1}, V_{dc2}) of two modules have the same value which is $40V_{DC}$. The modulation index and ST duty ratio are *0.847* and *0.153*, respectively. As a result, the RMS value of output voltage can be calculated as $110V_{RMS}$, approximately. The carrier frequency of V_{car1} and V_{car4} is 5 kHz whereas 15 kHz is the value of carrier frequency of V_{car2} and V_{car3}. The output voltage of the inverter is fed to resistor load (R=*40* Ω) through a low pass filter (L_f and C_f) to improve the quality of output load voltage

Table 1. Parameters used in simulation and experiment.

Parameter/Component		Value
Input voltage	V_{dc1}, V_{dc2}	*40V*
RMS output voltage	$V_{o,RMS}$	$110V_{RMS}$
Output frequency	f_o	*50Hz*
Carrier frequency	f_s	*5KHz, 15KHz*
Modulation index	M	*0.847*
ST duty ratio	D_0	*0.153*
Boost inductor	L_{x1}, L_{x2}	*3mH*
Boost capacitor	C_{x1}, C_{x2}	*2mF*
LC filter	L_f, C_f	*3mH, 10μF*
Resistor load	R	*40*Ω

Fig. 7 shows the simulation results for each module of the 5L-qSB-CHB. From top to bottom: input voltage (V_{dcx}), capacitor voltage (V_{Cxy}), inductor current (I_{Lxy}), DC-link voltage (V_{dc_linkx}), module output voltage (V_{Ox}) (x, y=*1, 2*).



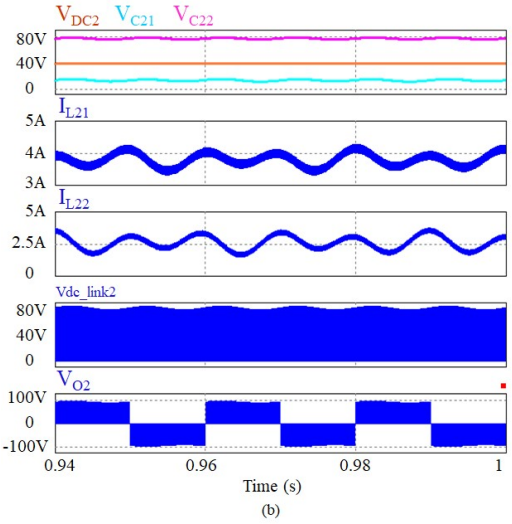


Figure 7. Simulation results for Input voltage (V_{dcx}), Capacitor voltage (V_{Cxy}), Inductor current (I_{Lxy}), DC-link voltage, Module output voltage ($V_{dc-linkx}$). a) module 1 b) module 2. (x, y=1, 2).

As illustrated in Fig. 7. From *40V* of input power supply, the capacitors C_{11} and C_{21} are boosted to *13.3V*, whereas the capacitors C_{12} and C_{22} are boosted to *77.3V*. As a result, the peak-value of DC-link voltage is *90V*, approximately. Therefore, the output voltage of each module has three-level voltage which are *+90V, 0V,* and *-90V*, as shown in Fig. 7. The average value of inductor current of L_{x1} and L_{x2} (x=*1, 2*) are *3.8A* and *2.6A*, respectively.

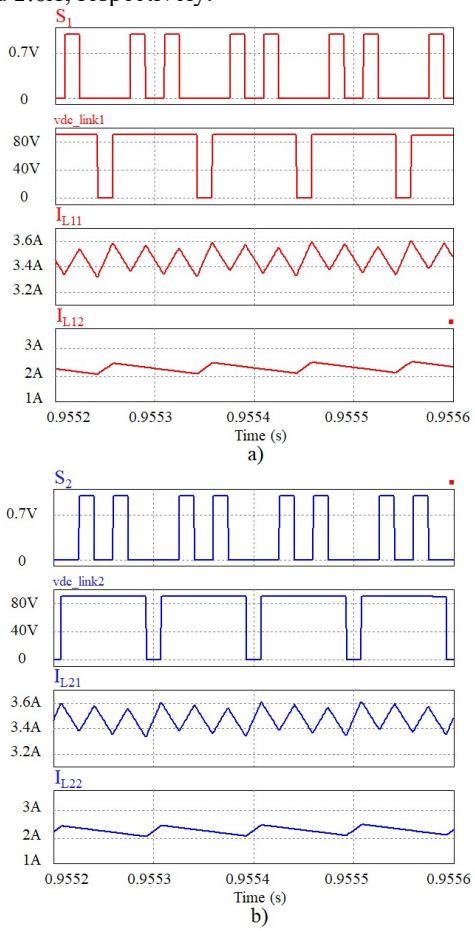


Figure 8. Simulation results for Control signal of Sx, DC-link voltage (Vdc-link), Inductor current (ILxy). a) module 1 b) module 2. (x,y=1,2).

The simulation results for switching control signal of Sx (x=1, 2), dc-link voltage, detailed about inductor current ripple of each module are presented in Fig. 8. Each module operates under NST 1 when the control signal of Sx is achieved "1". As a result, the inductor Lx1 is stored energy. Moreover, the Lx1 is also stored energy in ST mode when DC-link voltage is zero whereas the inductor Lx2 is just charged in ST mode, as shown in Fig. 8.

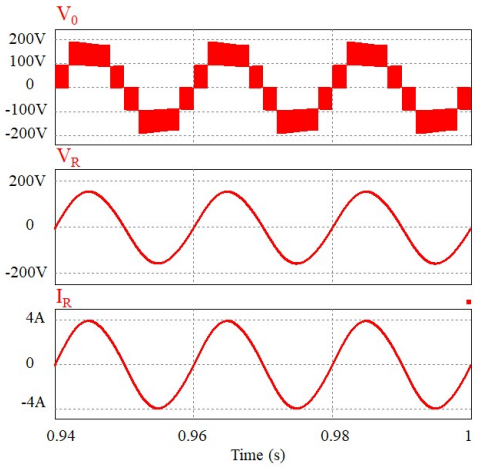


Figure 9. Simulation results for Output voltage (Vo), load voltage (VR) and load current (IR).

Fig. 9 shows the simulation results about output voltage (V_o), load voltage (V_R) and load current (I_R) of 5L-qSB-CHB. Each module of introduced topology produces three-level at output voltage, so the output voltage of 5L-qSB-CHB has five-level, which are measured from the simulation as *+180V, +90V, 0V, -90V, +180V*, approximately. Due to having a higher number of output voltage levels compared to [12], the output voltage quality is improved, significantly. The simulation result measures the THD of output voltage as *36.3%.* The RMS value of output load voltage and output load current are $110V_{RMS}$ and $2.76A_{RMS}$, respectively. Fig.10. shows the investigation about quality of output voltage of two topologies which are the proposed topology and topology proposed in [12]. As presented in Fig. 10, the THD value of output voltage of the proposed topology at the modulation index 0.75 is reduced over 50% compared with topology in [12]. In addition, by producing five-level voltage at output terminal, the quality of output voltage is significantly improved compared to [12], which just produces three-level voltage at output.

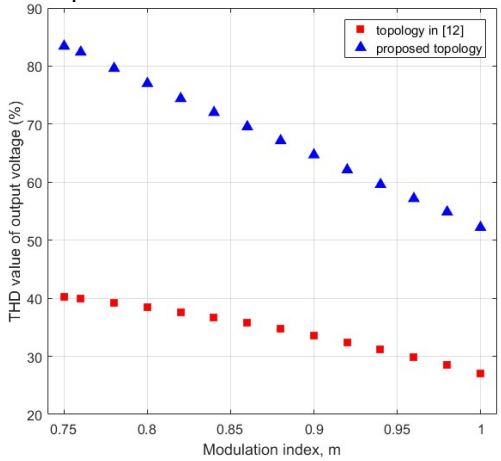


Figure 10. THD value of output voltage versus modulation index of proposed topology and topology in [12].

2.2.2. *Experimental results*

An experimental prototype is built in a laboratory to validate the performance of the introduced configuration. The parameter used in the experiment is the same as simulation and it is also listed in Tab. 2.

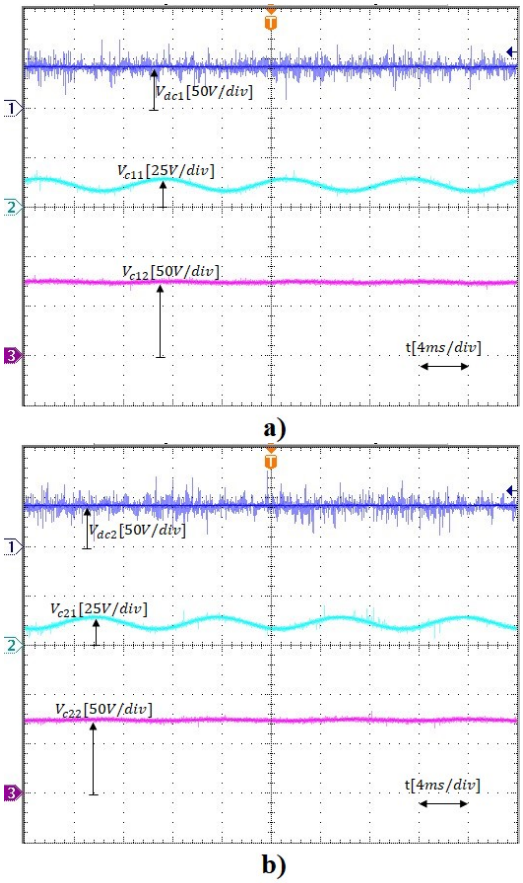
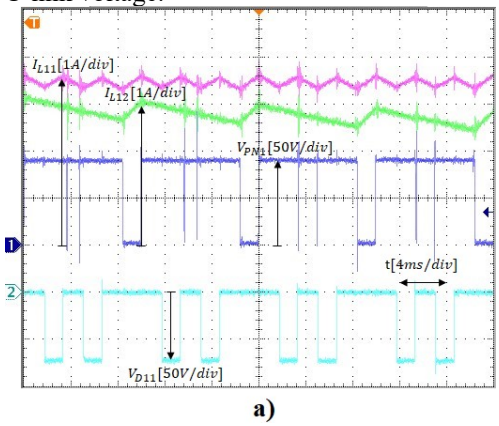
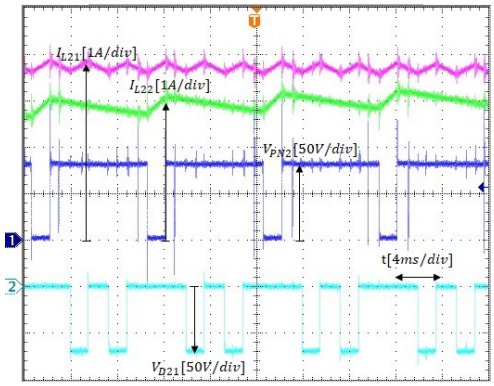


Figure 11. Experimental results for input voltage Vdcx, capacitor voltage Vcxy (x, y=1, 2). a) module 1, b) module 2.

Fig. 11 shows the input voltage and capacitors voltage of two modules. The experiment result measures the input power supply is *40V* for module 1 and module 2. Because of setting *0.153* for the ST duty ratio, the average value of capacitor voltages of C_{x1} and C_{x2} ($x=1, 2$) are *11V* and *74V*, respectively. As a result, the peak value of DC-link voltage (V_{PNx}) is *85V*, which is calculated by summing two capacitor voltages (V_{Cx1} and V_{Cx2}), as illustrated in Fig. 11. Moreover, this figure also shows that two inductors (L_{x1} and L_{x2}) are stored energy in ST mode, which is represented by zero value of DC-link voltage.





b)

Figure 12. Experimental results for inductor current ILxy, DC-link voltage VPNx and diode voltage VDx1 (x, y=1, 2). a) module 1, b) module 2.

The inductor L_{x1} is also charged when the switch S_x is triggered "ON", which is appeared when the diode D_{x1} is reverse-biased, as shown in Fig. 12.

Because the peak-value of the qSB network output is 85V, the output voltage of each module has three-levels which are +85V, 0V and -85V, approximately, as shown in Fig. 13. Furthermore, this figure also shows the inductors current in a period of the output voltage. As illustrated in Fig. 13, the inductor currents are not constant during the period of load voltage and their average value is 3.62A for ILx1 and 2.44A for ILx2.

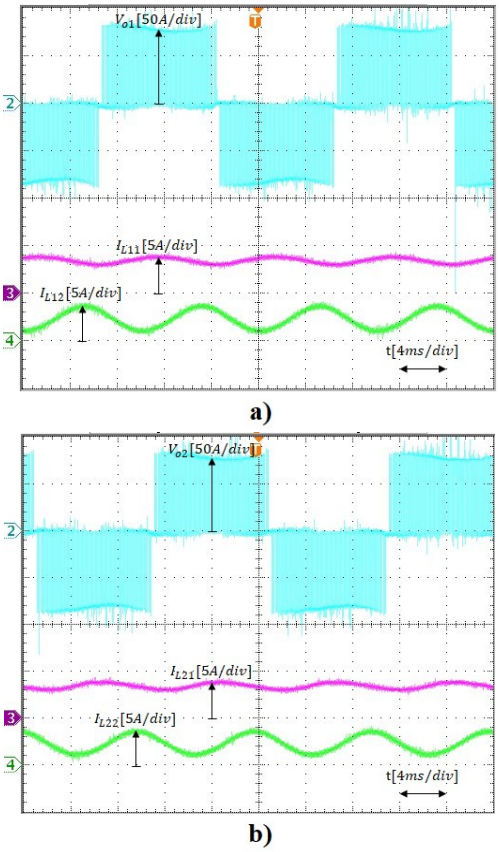


Figure 13. Experimental results for module output voltage V_{ox}, inductor current I_{Lxy} (x, y=1, 2). a) module 1, b) module 2.

Because there are three-level voltages at each module output, the output of the inverter has five-level which are *+170V, +85V, 0V, -85V,* and *-170V*, as presented in Fig. 12. Due to having a high number of output levels, the quality output voltage waveform is significantly improved, the THD value of output voltage is *37.5%* which is measured in the experiment. By applying the low pass filter at the output, the load voltage and load current have low THD value, as shown in Fig. 13 and the THD value of load current is *1.83%.* The RMS value of output load voltage and load current are $105V_{RMS}$ and $2.64A_{RMS}$, respectively.

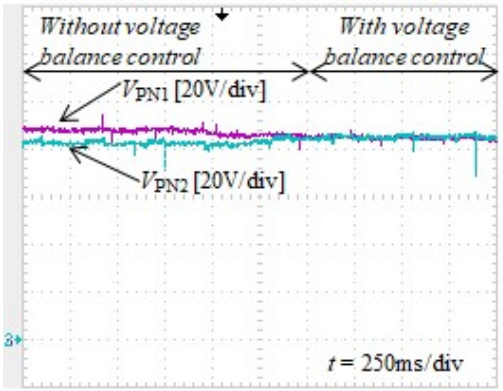


Figure 14. Experimental result of the V_{PN1} and V_{PN2}.

Fig. 14 shows the V_{PN1} and V_{PN2} with and without using the voltage-balance controller when V_{dc} = 40 V and V_{ph} = 110 Vrms. When the V_{PN1} and V_{PN2} -balance controller is applied to the 5L-qSB-CHB inverter, two DC-link voltages V_{PN1} and V_{PN2} are balanced with the same voltage of 85 V.

3. Conclusion

A new combination of quasi-switch boost networks and the five-level cascade inverter was proposed in this paper. The PWM control method was presented with some benefits such as 1) continuous input current, 2) reduced inductor current ripple, and 3) reduced voltage stress on power devices, and 4) shoot-through immunity. Simulations and experimental results were conducted to confirm the accuracy of the theoretical analysis. A laboratory prototype was built to verify the accuracy of the proposed inverter. Because of all benefits mentioned above, this configuration is suitable for low and medium voltage applications like photovoltaic systems or motor drives.

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