Small-signal analysis and PI controller design for a five-level modified quasi-Z-source H-bridge Inverter

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Abstract

This paper presents a single-phase five-level inverter topology using a modified quasi-Z-source network (Five-level Modified Quasi-Z-source H-bridge Inverter – 5L-MqZS-HBI), which combines two quasi-Z-source networks with an H-bridge inverter. 5L-MqZS-HBI is designed to reduce the number of inductors, improve overall efficiency, and enhance voltage gain while maintaining the ability to generate multilevel output voltages, making it suitable for applications requiring high-quality, high-voltage outputs with low harmonic distortion under low input voltage conditions. A small-signal analysis is performed considering parasitic elements of inductors and capacitors to establish the relationships between capacitor voltage, inductor current, and control parameter, so the system transfer function is derived to design a PI controller that ensures stable output voltage despite changes in input voltage or load. The paper also presents detailed operating states, evaluates controller performance, efficiency, and THD, and confirms the analysis through PSIM, MATLAB simulations and laboratory experiments.

***Keywords**: Small-signal analysis; PI controller; DQ Transformation*

Symbols

Symbols	Units	Description
$G(s)$		transfer function
K_P		proportional gain
K_I		integral gain
A, B		state space matrix

Abbreviations

PWM	pulse width modulation
PI	proportional-integral
LST	lower shoot-through
NST	non-shoot-through
UST	upper shoot-through
THD	total harmonic distortion

1. Introduction

Currently, within the framework of the energy crisis and the global pressure to mitigate greenhouse gas emissions, renewable energy sources are the most viable alternative to fossil fuels, owing to their environmental sustainability, low environmental impact, and diverse supply sources [1], [2]. Solar photovoltaic (PV) energy is among the most widely utilized forms of renewable energy. Nevertheless, renewable energy in general, and solar systems in particular, face the challenge of relatively low electricity output. Specifically, for a line of solar panels in a PV system, the output voltage typically ranges from tens to hundreds of volts and is affected by environmental conditions as well as panel aging [3]. To address this problem and ensure an alternative current (AC) applicable to loads and grid connections, conventional PV systems typically employ a two-stage power converter architecture [4], [5]: The first stage is a DC-DC boost converter, which is responsible for increasing the DC voltage to an appropriate level, and the second stage is a conventional Voltage Source Inverter (VSI), which converts the boosted DC voltage into an AC voltage with a sinusoidal waveform.

Although the two-stage architecture is easy to implement and deploy because each stage operates independently, it still has some limitations, such as increasing the overall system cost and causing additional power conversion losses. To overcome these limitations, the Z-source Inverter (ZSI) [6] and the quasi-Z-source Inverter (qZSI) [7] have been proposed and studied, in which the traditional DC-link is replaced by a Z-source impedance network. A distinctive feature of the ZSI/qZSI is its ability to boost the DC-link voltage directly within the inverter by utilizing the shoot-through (ST) state of the inverter bridge, which occurs only within a single power stage [8]. Additionally, multilevel inverters have been studied and demonstrated outstanding effectiveness in grid-connected and high-power applications, owing to their ability to generate a stepped approximation of sinusoidal voltage waveform, reduce THD, and decrease the voltage stress on each semiconductor device compared with two-level inverters [9].

Therefore, the combination of the boosting capability of the Z-source and the voltage quality of multilevel inverters offers several advantages for the system. However, several multilevel inverter topologies integrated with Z-source networks, such as Neutral-Point-Clamped quasi-Z-source Inverter (NPC-qZSI) [10] or quasi-Z-source Cascaded Multilevel Inverter (qZS-CMI) [11], still present certain limitations: the large number of inductors, capacitors, and diodes makes the configuration bulky and costly. Besides, particularly in terms of NPC-qZSI configuration, despite two similar impedance network qZSI, the boosting performance shows no improvement compared with the traditional qZSI. In the case of the qZS-CMI configuration, increasing the voltage level requires adding more stages, which consequently leads to an increase in circuit size.

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Thus, to reduce the number of components such as inductors and enhance the voltage boost, paper [12] has proposed a five-level single-phase configuration using an improved quasi-Z-source network (Five-level Modified Quasi-Z-source H-bridge Inverter – 5L-MqZS-HBI), which consists of two symmetric quasi-Z-source networks and an H-bridge inverter, aiming to generate a five-level voltage suitable for high-voltage applications with lower THD. An improved phase-shift modulation technique based on an alternately symmetric phase arrangement APOD (Alternate Phase Opposition Disposition) is proposed to improve the effectiveness of the ST state in order to boost the DC-link voltage. However, ensuring a more stable output voltage under varying load and input voltage conditions remains a challenging issue. This requires a closed-loop PI controller, which is widely used in many inverters [19].

In this paper, the research team conducts a small-signal analysis for the 5LMqZS-HBI configuration [12], considering parasitic components [13]. Based on small-signal analysis, the system transfer functions are derived, and their stability is evaluated using the Bode criterion. From this analysis, the PI controller parameters are determined to stabilize the system, improve both the phase margin and gain margin, and evaluate the performance as well as the THD under PI control. Based on the evaluation results, the DC-link voltage and the load voltage of the inverter are stabilized at the desired values, while both efficiency and THD are improved. Theoretical analysis, simulation results, and experimental verification with a resistive load are presented in this paper.

2. 5L-MqZS-HBI configuration

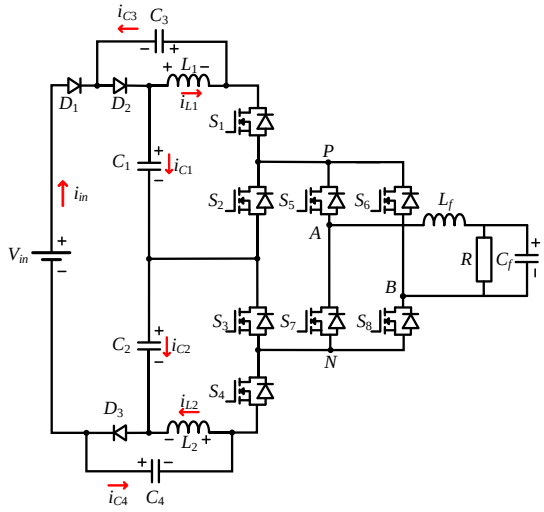


Figure 1: 5L-MqZS-HBI configuration [12].

5L-MqZS-HBI configuration is formed from the combination of a modified quasi-Z-source (MqZS) impedance network and a bridge inverter, as illustrated in Figure 1. Specifically, the proposed configuration consists of one DC source, eight semiconductor switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8), three diodes (D_1, D_2, D_3), three inductors (L_1, L_2, L_f), five capacitors (C_1, C_2, C_3, C_4, C_f), and a resistive load R. The MqZS network functions as a DC–DC converter that generates a three-level voltage at the V_{PN} output. This output, combined with an H-bridge inverter, generates a five-level voltage at the V_{AB} output. When passing through the LC filter, the output voltage across the load is smoothed into a sinusoidal waveform.

2.1 Operating state

The state of operation of the 5L-MqZS-HBI consists of six main operating modes, namely UST mode, LST mode, as well as four NST modes, denoted as NST-1, NST-2, NST-3, and NST-4. All of these are illustrated in Figure 2 and Table 1. The main waveforms and the PWM control algorithm of the configuration are illustrated in Figure 3 and Figure 4.

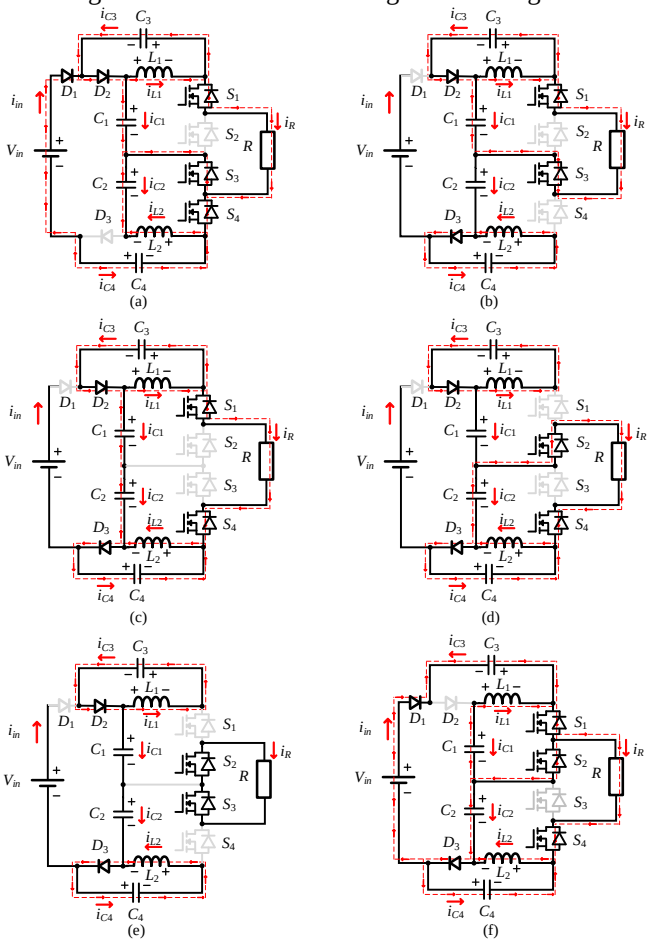


Figure 2: Operating states of the research configuration: (a) LST state, (b) NST-1 state, (c) NST-2 state, (d) NST-3 state, (e) NST-4 state, (f) UST state

Table 1: Operating states of 5L-MqZS-HBI

States	Turned-on semiconductor switch	Forward diode	V_{AB}
LST	S_1, S_3, S_4 (S_5, S_8 or S_6, S_7)	D_1, D_2	$\pm V_{PN} = V_{C1} + V_{C3}$
UST	S_1, S_2, S_4 (S_5, S_8 or S_6, S_7)	D_1, D_3	$\pm V_{PN} = V_{C2} + V_{C4}$
NST- 1	S_1, S_3 (S_5, S_8 or S_6,S_7)	D_2, D_3	$\pm V_{PN} = V_{C1} + V_{C3}$
NST- 2	S_1, S_4 (S_5, S_8 or S_6, S_7)	D_2, D_3	$\pm V_{PN} = V_{C1}+V_{C2}+V_{C3}+V_{C4}$
NST- 3	S_2, S_4 (S_5, S_8 or S_6, S_7)	D_2, D_3	$\pm V_{PN} = V_{C2} + V_{C4}$
NST- 4	S_2, S_3 (S_5, S_8 or S_6, S_7)	D_2, D_3	$\pm V_{PN} = 0$

Stage 1 [$t_0 - t_1$, illustrated in Figure 3(a) and Figure 3(b)] corresponds to the LST state shown in Figure 2(a). Semiconductor switches S_1, S_3, and S_4 are turned on, while

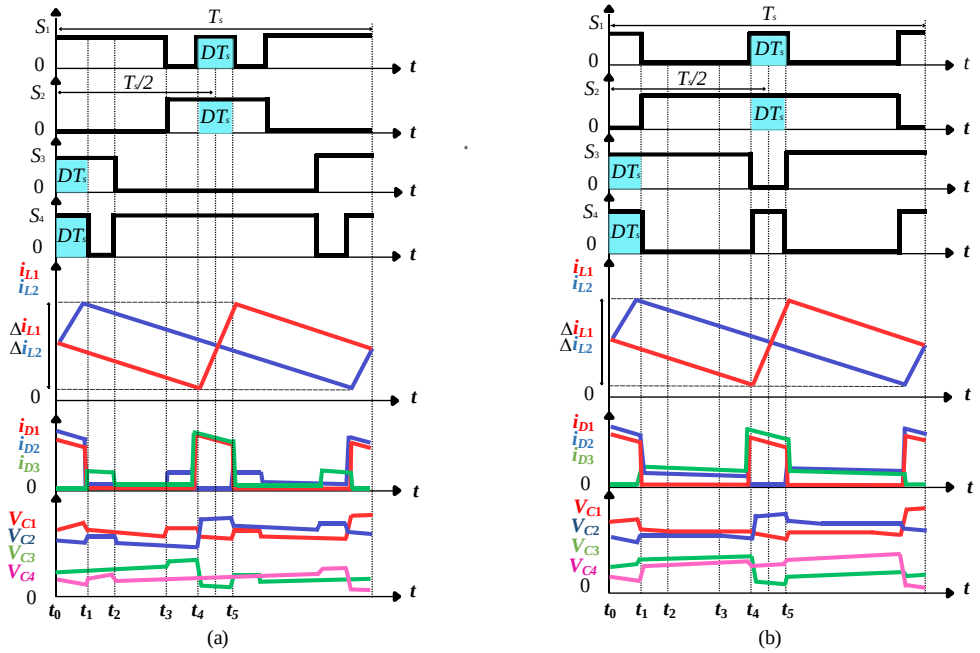


Figure 3: Waveforms of the 5L-MqZS-HBI: (a) $V_{ref} \geq 0.5$, (b) $V_{ref} < 0.5$.

switch S_2 is turned off. At the same time, diodes D_1 and D_2 are forward-biased, whereas diode D_3 is reverse-biased. Capacitors C_2 and C_4 discharge, whereas capacitors C_1 and C_3 charge.

Stage 2 [$t_1 - t_2$, illustrated in Figure 3(a) and Figure 3(b)] corresponds to the NST-1 state illustrated in Figure 2(b). Switches S_1 and S_3 are turned on, while switches S_2 and S_4 are turned off. At the same time, diodes D_2 and D_3 are forward-biased, whereas diode D_1 is reverse-biased. Besides, inductors L_1 and L_2 release energy, capacitor C_1 discharges, capacitors C_3 and C_4 charge, while capacitor C_2 does not participate in energy exchange.

Stage 3 [$t_2 - t_3$, illustrated in Figure 3(a)] corresponds to the NST-2 state shown in Figure 2(c). Switches S_1 and S_4 are turned on, while switches S_2 and S_3 are turned off. At the same time, diodes D_2 and D_3 are forward-biased, whereas diode D_1 is reverse-biased. Meanwhile, inductors L_1 and L_2 release energy, capacitors C_1 and C_2 discharge, while capacitors C_3 and C_4 charge.

Stage 4 [$t_3 - t_4$, illustrated in Figure 3(a) and Figure 3(b)] corresponds to the NST-3 state illustrated in Figure 2(d). Switches S_2 and S_4 are turned on, while switches S_1 and S_3 are turned off. Simultaneously, diodes D_2 and D_3 are forward-biased, whereas diode D_1 is reverse-biased. Meanwhile, inductors L_1 and L_2 release energy, capacitor C_2 discharges, and capacitors C_3 and C_4 charge. Capacitor C_1 does not participate in energy exchange.

Stage 5 [$t_4 - t_5$, illustrated in Figure 3(a) and Figure 3(b)] corresponds to the UST state shown in Figure 2(f). Switches S_1, S_2, and S_4 are turned on, while switch S_3 is turned off. Simultaneously, diodes D_1 and D_3 are forward-biased, whereas diode D_2 is reverse-biased. Meanwhile, inductor L_1 stores energy and inductor L_2 releases energy. Capacitors C_1 and C_3 discharge, while capacitors C_2 and C_4 charge.

Stage 6 [$t_2 - t_3$, illustrated in Figure 3(b)] is NST-4 state illustrated in Figure 2(e). Switches S_2 and S_3 are turned on, while switches S_1 and S_4 are turned off. At the same time, diodes D_2 and D_3 are forward-biased and diode D_1 is reverse-biased. Meanwhile, inductors L_1 and L_2 release energy, capacitors C_3 and C_4 discharge, capacitors C_1 and C_2 do not participate in energy exchange.

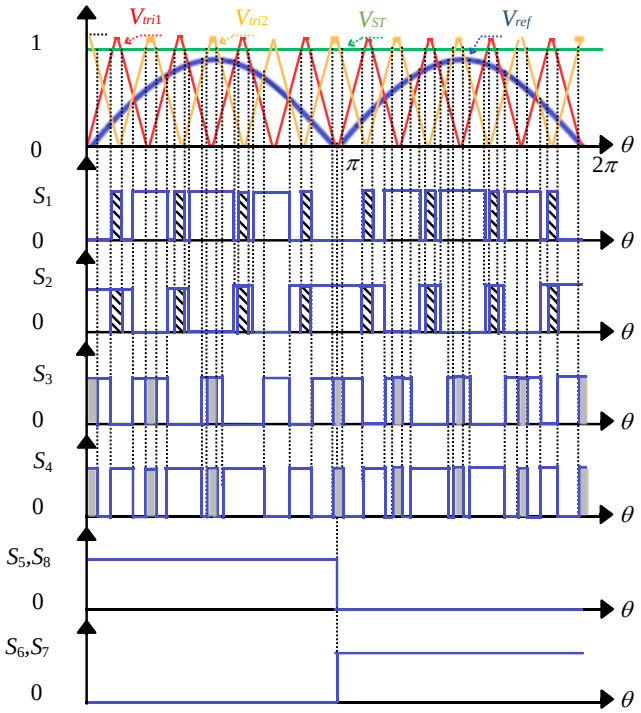


Figure 4: Control algorithm.

Based on the above stage analysis, the voltage equations across the inductors are obtained as follows:

$$\begin{cases} \int_{t_0}^{t_1} V_{L1}(t)\,dt = (-V_{C3})(DT) \\ \int_{t_4}^{t_5} V_{L1}(t)\,dt = (-V_{in} - V_{C3} + V_{C1} + V_{C2})(DT) \\ \int_{2DT}^{T} V_{L1}(t)\,dt = (-V_{C3})(T - 2DT) \end{cases} \quad (1)$$

2.2 Steady-state analysis

From equation (1), applying the inductor voltage-second balance principle, the capacitor voltage equations are derived as follows:

$$\begin{cases} V_{C1} = V_{C2} = \dfrac{1-D}{(1-2D)} V_{in} \\ V_{C3} = V_{C4} = \dfrac{D}{(1-2D)} V_{in} \end{cases} \tag{2}$$

The boost factor B, the load peak voltage $V_{R,peak}$, and the voltage gain G are calculated as follows:

$$\begin{cases} B = \dfrac{V_{PN,peak}}{V_{in}} = \dfrac{V_{C1}+V_{C2}+V_{C3}+V_{C4}}{V_{in}} = \dfrac{2}{1-2D} \\ V_{R,peak} = MV_{PN,peak} = MV_{in}\dfrac{2}{1-2D} \\ G = \dfrac{V_{R,peak}}{V_{in}} = M\dfrac{2}{1-2D} \end{cases} \tag{3}$$

3. Small-signal analysis, transfer function derivation and PI controller design

3.1 Small-Signal analysis and transfer functions of the 5L-MqZS-HBI configuration

Using the state-space averaging method [7], the state-space expression is presented in (4). Moreover, the equivalent model of the configuration is illustrated in Figure 5 using the equivalent modeling approach [17] and added parasitic components [13]:

$$\begin{cases} \dfrac{dx}{dt} = Ax + Bu \\ x = \left[i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}\ v_{C3}\ v_{C4} \right]^T \\ u = \left[v_{in}\ i_R \right]^T \end{cases} \tag{4}$$

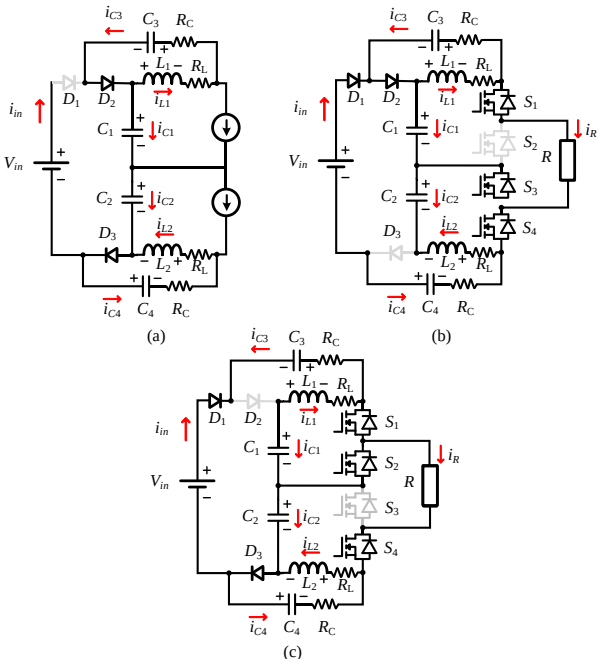


Figure 5: The main operating states of the configuration, including parasitic components, are as follows: (a) equivalent configuration of the NST states, (b) LST state, (c) UST state.

Equation (4), in which we obtain:

$$\begin{cases} A = A_{UST}d + A_{LST}d + (1-2d)A_{NST} \\ B = B_{UST}d + B_{LST}d + (1-2d)B_{NST} \end{cases} \tag{5}$$

$$A_{LST} = \begin{bmatrix} -\dfrac{(R_L+R_C)}{L} & 0 & 0 & 0 & -\dfrac{1}{L} & 0 \\ 0 & -\dfrac{R_L}{L} & 0 & \dfrac{1}{L} & 0 & 0 \\ 0 & 0 & -\dfrac{1}{R_C C} & 0 & 0 & \dfrac{1}{R_C C} \\ 0 & -\dfrac{1}{C} & 0 & 0 & 0 & 0 \\ \dfrac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{1}{R_C C} & 0 & 0 & -\dfrac{1}{R_C C} \end{bmatrix} \tag{6}$$

$$A_{UST} = \begin{bmatrix} -\dfrac{R_L}{L} & 0 & \dfrac{1}{L} & 0 & 0 & 0 \\ 0 & -\dfrac{(R_L+R_C)}{L} & 0 & 0 & 0 & -\dfrac{1}{L} \\ -\dfrac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\dfrac{1}{R_C C} & \dfrac{1}{R_C C} & 0 \\ 0 & 0 & 0 & \dfrac{1}{R_C C} & -\dfrac{1}{R_C C} & 0 \\ \dfrac{1}{C} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{7}$$

$$A_{NST} = \begin{bmatrix} -\dfrac{(R_L+R_C)}{L} & 0 & 0 & 0 & -\dfrac{1}{L} & 0 \\ 0 & -\dfrac{(R_L+R_C)}{L} & 0 & 0 & 0 & -\dfrac{1}{L} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \dfrac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & \dfrac{1}{C} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{8}$$

$$B_{LST} = \begin{bmatrix} 0 & \dfrac{R_C}{L} \\ 0 & 0 \\ \dfrac{1}{R_C C} & -\dfrac{1}{C} \\ 0 & 0 \\ 0 & -\dfrac{1}{C} \\ -\dfrac{1}{R_C C} & 0 \end{bmatrix} B_{UST} = \begin{bmatrix} 0 & 0 \\ 0 & \dfrac{R_C}{L} \\ 0 & 0 \\ \dfrac{1}{R_C C} & -\dfrac{1}{C} \\ -\dfrac{1}{R_C C} & 0 \\ 0 & -\dfrac{1}{C} \end{bmatrix}; B_{NST} = \begin{bmatrix} 0 & \dfrac{R_C}{L} \\ 0 & \dfrac{R_C}{L} \\ 0 & -\dfrac{1}{C} \\ 0 & -\dfrac{1}{C} \\ 0 & \dfrac{1}{C} \\ 0 & \dfrac{1}{C} \end{bmatrix} \tag{9}$$

To model the small-signal response of the 5L-MqZS-HBI, each signal is decomposed into its DC and AC components [7]. Specifically, $x = X + \hat{x}$ (in which X denotes the DC component, and $\hat{x}$ represents the small-signal perturbation $x = d,\ i_{L1}, i_{L1}, v_{C1}, v_{C2}, v_{C3}, v_{C4},\ v_{in},\ i_R$).

Replacing $x = X + \hat{x}$, from equation (4):

$$\underbrace{\frac{dX}{dt}}_{0\text{th}}+\underbrace{\frac{d\hat{x}}{dt}}_{1\text{st}}=\underbrace{f(X)}_{0\text{th}}+\underbrace{f(X*\hat{x})}_{1\text{st}}+\underbrace{f(X*\hat{x}*\hat{x})}_{2\text{nd}} \quad (10)$$

The zeroth-order component is eliminated (because it is a DC component) and the second-order component is also eliminated (because it is negligibly small, approximately zero). Additionally, $\hat{v}_{in}=0$ (for all inputs, the output remains unchanged), $\hat{i}_R=0$ (the i_R remains constant for all loads).

Based on equation (10) and the statistical data shown in Table 2, the transfer function is derived as follows: $\hat{v}_{PN}/\hat{d}=(\hat{v}_{C1}+\hat{v}_{C2}+\hat{v}_{C3}+\hat{v}_{C4})/\hat{d}$.

$$\frac{\hat{v}_{C1}}{\hat{d}}\Big|_{\hat{i}_R=0,\hat{v}_{in}=0}^{\hat{i}_R=0}=\frac{\hat{v}_{C2}}{\hat{d}}\Big|_{\hat{v}_{in}=0}^{\hat{i}_R=0}=-\frac{1.74\times10^4 s^2+5.1007\times10^8 s-4.4976\times10^{11}}{3s^3+2.414\times10^4 s^2+1.8\times10^6 s+1.44\times10^9} \quad (11)$$

$$\frac{\hat{v}_{C3}}{\hat{d}}\Big|_{\hat{i}_R=0,\hat{v}_{in}=0}^{\hat{i}_R=0}=\frac{\hat{v}_{C4}}{\hat{d}}\Big|_{\hat{v}_{in}=0}^{\hat{i}_R=0}=-\frac{9.99\times10^4 s^2+3.1363\times10^8 s-4.5654\times10^{11}}{3s^3+2.414\times10^4 s^2+1.8\times10^6 s+1.44\times10^9} \quad (12)$$

$$G_{vd}(s)=\frac{\hat{v}_{PN}}{\hat{d}}=-\frac{2.346\times10^5 s^2+1.6474\times10^9 s-1.8126\times10^{12}}{3s^3+2.414\times10^4 s^2+1.8\times10^6 s+1.44\times10^9} \quad (13)$$

Table 2: Component parameters

Components	Parameters
L_1, L_2	3mH, 0.1Ω
C_1, C_2, C_3, C_4	1mF, 0.05Ω
V_{in}	120V
D	0.2

3.2 Small-signal analysis and transfer functions of the filter

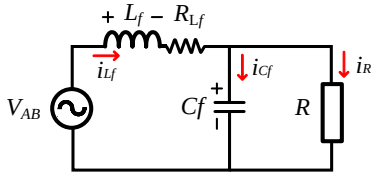


Figure 6: The LC filter, considering the parasitic components of the inductor.

Applying the Park transformation [15], the signals are converted from the $\alpha\beta$ domain to the dq domain according to the following formula:

$$\begin{bmatrix}v_d\\v_q\end{bmatrix}=\begin{bmatrix}\cos(\theta) & \sin(\theta)\\-\sin(\theta) & \cos(\theta)\end{bmatrix}\begin{bmatrix}v_\alpha\\v_\beta\end{bmatrix} \quad (14)$$

$$\begin{cases}v_\alpha(t)=V_M\sin(\theta)\\v_\beta(t)=V_M\sin(\theta-\frac{\pi}{2})=-V_M\cos(\theta)\end{cases} \quad (15)$$

in which: V_M is peak value, θ is the phase angle.

As illustrated in Figure 6, the voltage and current equations are derived:

$$\frac{di_{Lf}}{dt}=\frac{v_{AB}}{L_f}-\frac{v_{Cf}}{L_f}-\frac{i_{Lf}R_{Lf}}{L_f};\quad \frac{dv_{Cf}}{dt}=\frac{i_{Lf}}{C_f}-\frac{i_R}{C_f} \quad (16)$$

From equations (14) and (16), and based on the small-signal analysis [7], the transfer functions are defined as follows:

$$G_{v_{Cf}i_{Lf}x}(s)=\frac{\hat{v}_{Cf}}{\hat{i}_{Lf}}=\frac{1}{sC_f};\ G_{i_{Lf}v_{refx}}(s)=\frac{\hat{i}_{Lf}}{\hat{v}_{ref}}=\frac{V_{PN}}{R_{Lf}+L_f s} \quad (17)$$

in which: $x=d,q$.

3.3 PI controller design

As illustrated in Figure 4 and Figure 7, the PWM control algorithm is employed to generate the switching signals for the semiconductor devices of the proposed configuration. To implement this control strategy, the modulation signals V_{ref}, and V_{ST} are defined as follows:

$$V_{ref}=\begin{cases}M*\sin(\theta), & \text{khi } 0\le\theta<\pi\\-M*\sin(\theta), & \text{khi } \pi\le\theta<2\pi\end{cases} \quad (18)$$

$$V_{ST}=1-D \quad (19)$$

in which: θ is the phase angle of the output voltage, M is the modulation index, D is the duty cycle, and $M + D \le 1$.

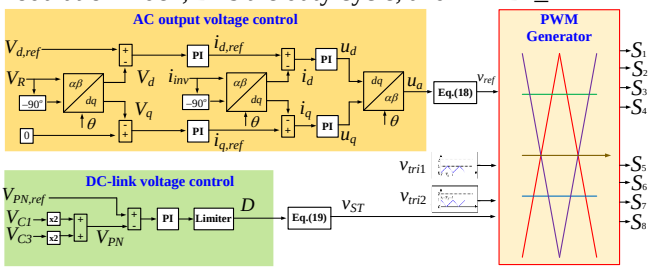


Figure 7: Control diagram of the DC bus voltage and AC output voltage.

The formula of the PI controller is expressed as follows, and the values of K_P and K_I are calculated according to the following equations:

$$G_{PI}(s)=K_P\left(1+\frac{K_I}{s}\right) \quad (20)$$

$$\begin{cases}K_I=\tan(180-PM+PHS)\times\omega_c\\K_P=\dfrac{1}{|G_{vd}(j\omega_c)|\times\sqrt{1+\left(\dfrac{K_I}{\omega_c}\right)^2}}\end{cases} \quad (21)$$

The phase margin (PM) directly affects the overshoot, transient time, response time, and the ability of the system to maintain stability. Therefore, to ensure stable operation and satisfactory performance, the PM should be selected in the range of 45° to 60° [16]. With the selected PM value is 60°, the PHS value must select within the ranges [-120° ; -30°], [60°; 150°] or [240°; 330°] since values outside these interval will result in $K_I < 0$.

3.3.1 *PI controller design for the transfer function of the 5L-MqZS-HBI configuration*

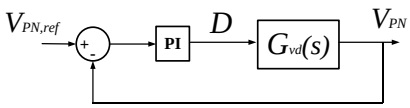


Figure 8: V_{PN} voltage control structure.

As illustrated in Figure 8, the V_{PN} voltage is fed back and compared with the reference voltage $V_{PN,\ ref}$ [18]. The resulting error is then processed by the PI controller to generate the control signal D. As shown in Figure 9, the closed-loop transfer function $G_{vd}(s)$ is unstable because of ($GM < 0$ and $PM < 0$) according to the Bode criterion. With the PI controller, the closed-loop transfer function $G_{vd}(s)$ becomes stable, with GM =11.7(dB) and PM=60° at a cut-off frequency ω_c= 250 (rad/s), which is much lower than the cut-

off frequency without the PI controller. This effectively reduces high-frequency noise in the system [14].

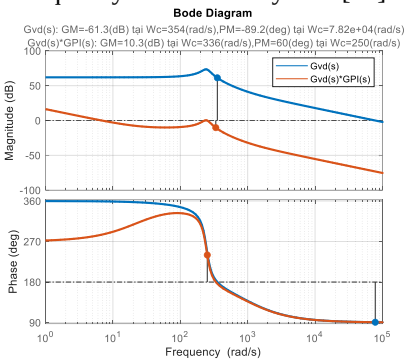


Figure 9: Bode diagram of the G_{vd} transfer function before and after the controller is applied.

3.3.2 PI controller design for the filter transfer function

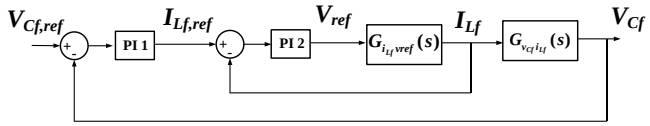
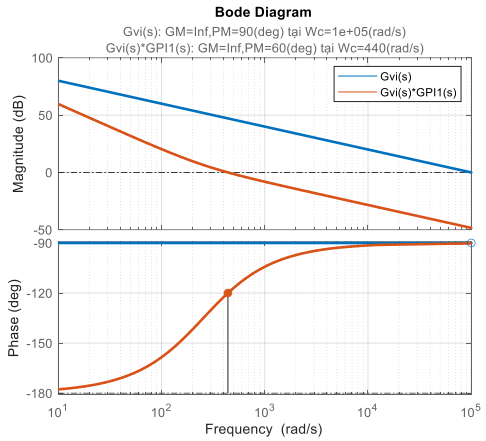
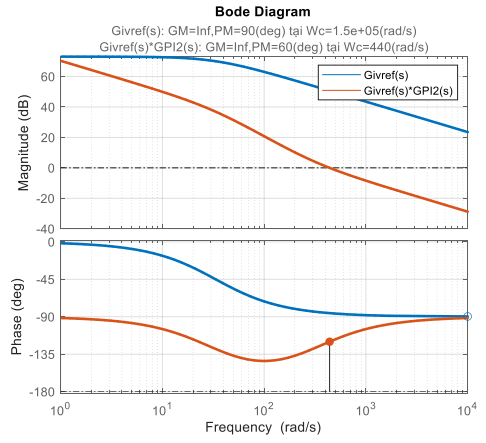


Figure 10: Two-loop voltage control structure on the capacitor



(a)



(b)

Figure 11: Bode diagram of the filter transfer function before and after the controller is applied: (a) $G_{v_{Cf}i_{Lf}}(s)$, (b) $G_{i_{Lf}v_{ref}}(s)$

As illustrated in Figure 10, the V_{Cf} voltage is fed back and compared with the reference voltage $V_{Cf,ref}$ [18]. The resulting error is processed by a PI controller to generate the reference current $I_{Lf,ref}$. Meanwhile, the I_{Lf} current is also fed back and compared with $I_{Lf,ref}$, and the resulting error is processed by another PI controller to generate the control signal V_{ref}. As shown in Figure 11, although the two closed-loop transfer functions of the filter are stable, their cut-off frequency ω_c is too high, allowing high-frequency noise to pass through. With the PI controllers, the closed-loop transfer functions achieve GM =Inf and PM=60° at a cut-off frequency ω_c=440 (rad/s), effectively reducing high-frequency noise and stabilizing the system.

4. Simulation results and evaluation of the controller

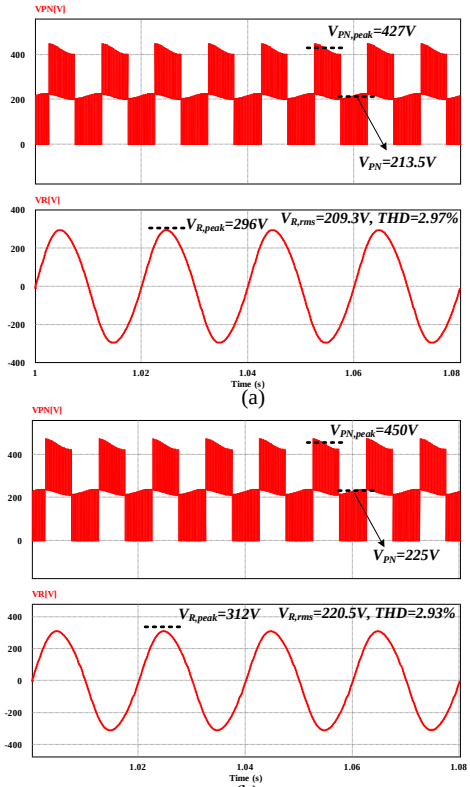


Figure 12: V_{PN} and V_R voltages at V_{in}=120V and P_{out} =1.6 kW considering the parasitic components: (a) without the controller, (b) with the controller.

At a fixed V_{in}=120V and a fixed P_{out}=1.6kW, the V_{PN} and V_R voltages of the configuration considering the parasitic components are shown in Figure 16. Specifically, with fixed M and D values calculated from equations (2) and (3) when V_{PN} is chosen at 450V, the three-level V_{PN} output voltages are 427V, 213.5V, and 0V, with $V_{R,rms}$=209.3V, THD=2.97%, and $V_{R,max}$=296V as illustrated in Figure 12(a). These values do not meet the desired output due to the occurrence of parasitic components. In contrast, with the PI controller when $V_{PN,ref}$ is set at 450V, the three-level V_{PN} output voltages are 450V, 225V, and 0V, with $V_{R,rms}$=220.5V, THD=2.93%, and $V_{R,max}$=312V, achieving the desired output, as shown in Figure 12(b). Consequently, the THD of the controlled method is improved by 0.04% compared with the uncontrolled method.

As shown in Figure 14(a), when V_{in} varies from 100V to 180V at a fixed output power of 1 kW, the capacitor voltagesand inductor currents also vary to maintain the output voltage thanks to the controller. The largest V_{in} variation is

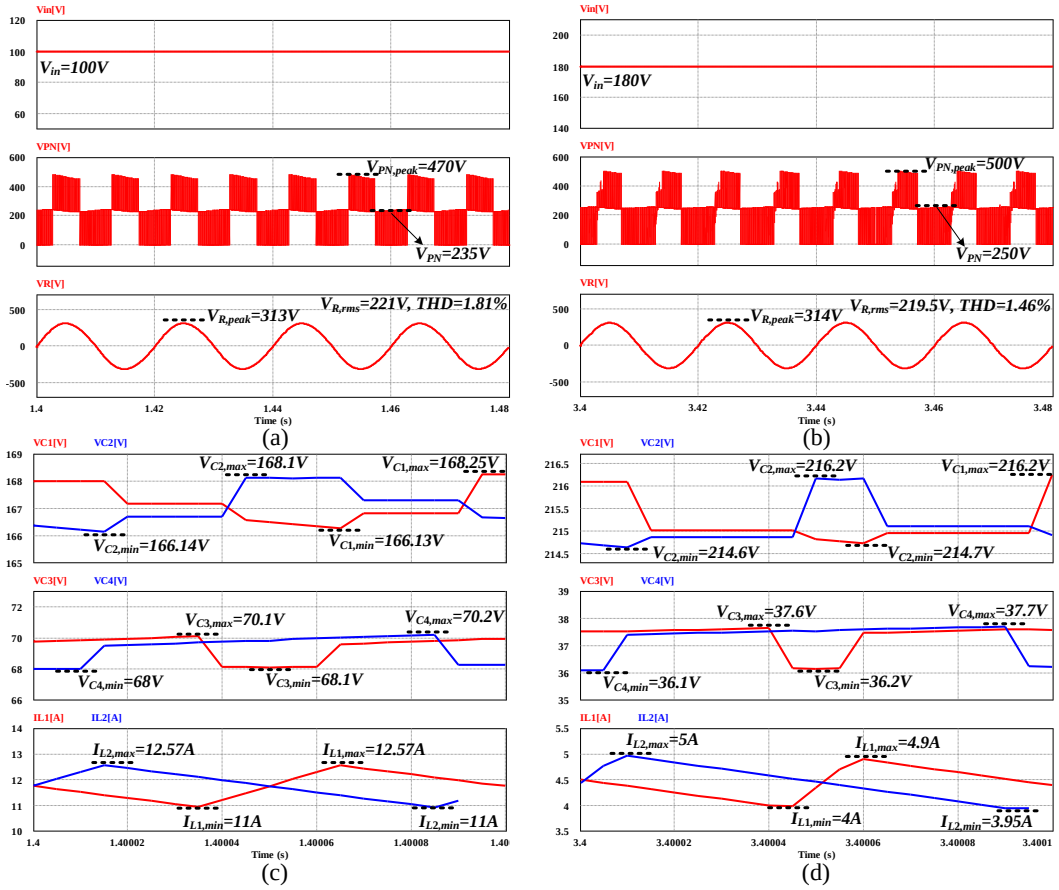


Figure 13: Steady-state V_{PN} and V_R voltages at P_{out}=1kW: (a) V_{in}=100V, (b) V_{in} =180V. Capacitor voltage and inductor current during one switching cycle, (c) V_{in}=100V, (d) V_{in}=180V.

illustrated in Figure 14(b), which causes V_{C1}, V_{C2} to increase from 172V to 213.5V; V_{C3}, V_{C4} to decrease from 53.4V to 36V; and I_{L1}, I_{L2} to decrease from 8.77A to 5.5A, with a settling time of 0.35s.

The reference $V_{PN,ref}$ is automatically adjusted during operation so that the system can adapt a wide range of V_{in} and satisfy $M+D \leq 1$. Combined with the PI controller, the steady-state voltages of V_{PN} and V_R are illustrated in Figure 13(a) and Figure 13(b), respectively. At the minimum V_{in}=100V and $V_{PN,ref}$ =470V, the three-level V_{PN} output voltages are 470V, 235V, and 0V, with $V_{R,rms}$=221V and THD=1.81%. At the maximum V_{in}=180V and $V_{PN,ref}$ =500V, the three-level V_{PN} output voltages are 500V, 250V, and 0V. Additionally, as shown in Figure 13(c) and Figure 13(d), the capacitors charge and discharge with a voltage ripple of around 1-2V and the inductors store and release energy with a current ripple of 1-2A.

As shown in Figure 16(a), when P_{out} varies from 0.86 to 1.7 kW at a fixed V_{in}=120 V and a fixed $V_{PN,ref}$ =450V, the capacitor voltages and inductor currents also vary to maintain the output voltage thanks to the controller. The largest P_{out} variation is illustrated in Figure 16(b), which shows that the voltages across the four capacitors remain almost unchanged, while I_{L1}, I_{L2} increase from 11.82A to 15.3A with a settling time of 0.34s.

The steady-state voltages of V_{PN} and V_R are shown in Figure 15(a) and 15(b). For the smallest P_{out}=0.86kW, the three-level V_{PN} output voltages are 450V, 225V, and 0V, with $V_{R,rms}$=219.1V, THD=1.83%, and $V_{R,peak}$=310.6V. Similarly, for the largest P_{out}=1.7kW, the three-level V_{PN} voltage is 450V, 225V, and 0V, with $V_{R,rms}$=219.9V, THD=3.12%, and $V_{R,peak}$=311V. Moreover, as illustrated in Figure 15(c) and Figure 15(d), the capacitors charge and discharge with a voltage ripple of 2-3V, and the inductors store and release energy with a current ripple of 1-2A.

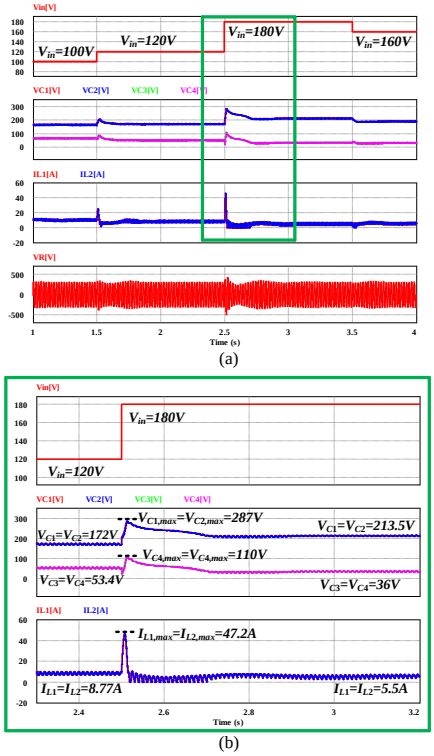


Figure 14: Capacitor voltage and inductor current when the input voltage varies using PI controller: (a) V_{in} from 100-180 V, (b) V_{in} from 120-180 V.

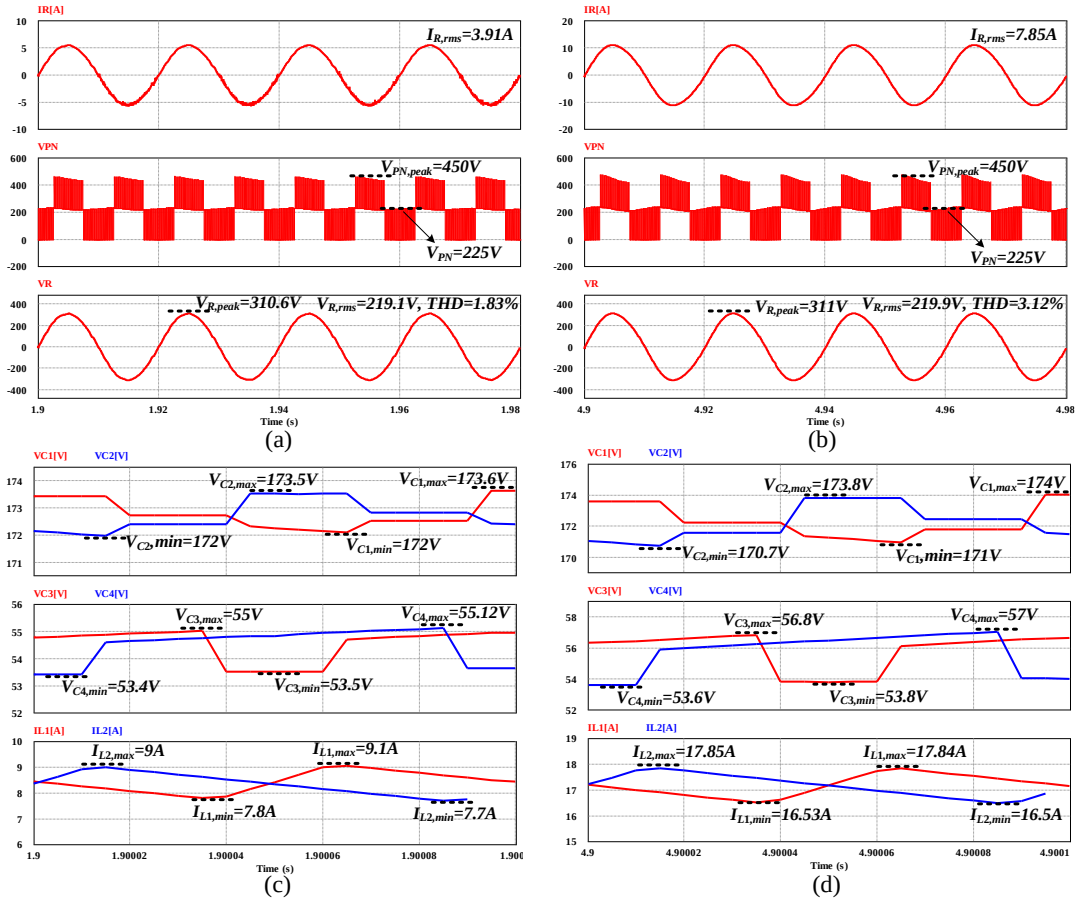


Figure 15: Steady-state V_{PN} and V_R voltages at V_{in}=120 V: (a) P_{out}=0.86 kW, (b) P_{out}=1.7 kW. Capacitor voltages and inductor currents during one switching cycle: (c) P_{out}=0.86 kW, (d) P_{out}=1.7 kW.

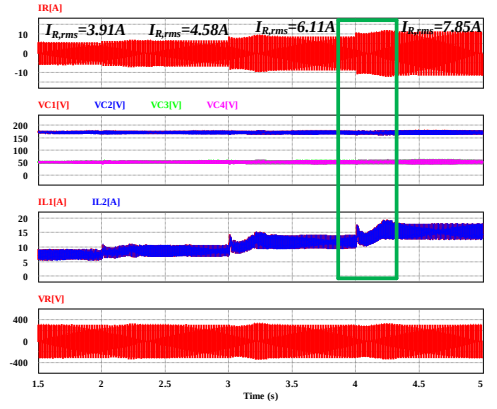


Figure 16. Capacitor voltage and inductor current under varying output power using PI controller: (a) P_{out} from 0.86-1.7kW, (b) P_{out} from 1.3-1.7kW.

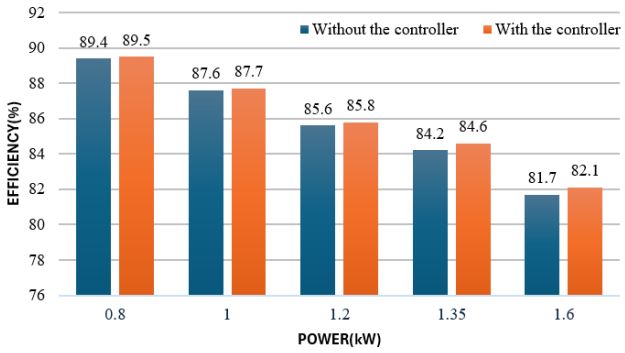


Figure 17. Comparison of efficiency over the power range with and without the controller.

From the efficiency analysis results for load powers of 0.8–1.6kW, as shown in Figure 17, the configuration exhibits decreasing efficiency as the power increases from 0.8 to 1.6kW (from 89.5% to 82.1% with the controller). At all measured power points, the efficiency of the method with the controller is higher than that of the method without the controller by an average of 0.24 %. Overall, it can be observed that using the controller improves efficiency compared with the uncontrolled method.

5. Experimental results

Figure 18 presents the experimental configuration setup and the component parameters listed in Table 3. A FPGA Cyclone II EP2C5T144C8 and a DSP TSM320F28379D are used to generate control signals for switches.

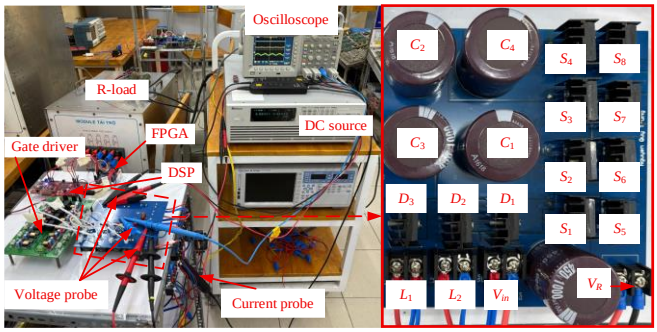


Figure 18: Experimental setup.

Table 3: Experimental parameters

Components	Parameters
V_{in}	150V
f_O	50Hz
f_S	10kHz
L_1, L_2	3mH/20A
C_1, C_2, C_3, C_4	1mF/450V
L_f and C_f	3mH and 10μF
R	72Ω
S_1, S_2 S_3, S_4	MOSFETs
S_5, S_6, S_7, S_8	C3M0075120K

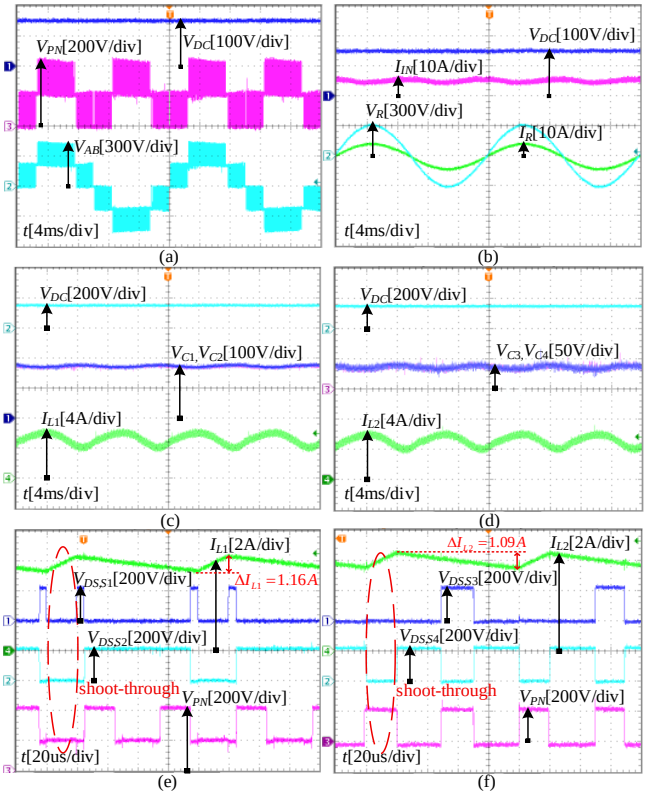


Figure 19: The experimental result of 5L-MqZS-HBI configuration at 150V input voltage without the controller

With V_{in}=150V, D=0.19 and M=0.7, the three-level V_{PN} output voltages are approximately 443V, 221V, and 0V, and the five-level V_{AB} output voltages are obtained through S_5, S_6, S_7, and S_8 operation, illustrated in Figure 19(a). In Figure 19(b), voltage and current input values are measured at 150V and 4.96A, respectively. Meanwhile, voltage and current output values are measured at 218V_{RMS} and 3A_{RMS}, in that order.

As shown in the experimental results of Figure 19(c), the average voltages of V_{C1} and V_{C2} are balanced at roughly 186V and 185V, respectively. Similarly, in Figure 19(d), the voltages of V_{C3} and V_{C4} are around 35.9V and 36.4V, indicating that these capacitor voltages are balanced.

As shown in the experimental results of Figure 19(e), when switches S_1 and S_2 are simultaneously turned on, the inductor L_1 is charged with a current ripple of 1.16 A, while its average current I_{L1} reaches 6.15A. Similarly, in Figure 19(f), when switches S_3 and S_4 are simultaneously turned on, the inductor L_2 is charged with a current ripple of 1.09 A and an average current I_{L2} of 6.31A. At the shoot-through state in both Figure 19(e) and Figure 19(f), it can be observed that inductors L_1 and L_2 start storing energy during the interval DT_s and release energy when the circuit is in non-shoot-through states. This demonstrates that the circuit operates consistently with the theoretical analysis.

6. Conclusion

This paper has presented the operating principle, small-signal analysis, and transfer function formulation of the 5L-MqZS-HBI circuit. The PI controller parameters were selected based on the analyzed transfer function. Simulation results on an R load demonstrated that the 5L-MqZS-HBI circuit with the proposed controller can regulate the desired load voltage despite variations in the input voltage, load conditions or output power, and parasitic components. In addition, the controlled configuration maintains higher efficiency and improves THD compared with the uncontrolled case within the investigated power range. These results lay the foundation for further development of the 5L-MqZS-HBI circuit for PV systems. Finally, experimental results on the laboratory prototype are indicated in section 5.

Acknowledgement

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