An improved structure for reducing parasitic capacitances in planar transformers for LLC resonant converters

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Abstract

This study investigates the design of a planar transformer for a 48V/3A electric motorcycle charger utilizing an LLC resonant converter. While planar transformers with PCB windings offer advantages such as compact size and high power density, they are hindered by high parasitic capacitances, including intra- and inter-winding types, which degrade voltage regulation, soft-switching efficiency, and cause issues with electromagnetic interference (EMI). Existing strategies, such as shielding layers, split-turn windings, and zero common-mode current (ZCC) layouts, effectively reduce specific parasitic capacitances but fail to address both intra- and inter-winding capacitances simultaneously. To overcome these limitations, this study proposes an improved winding layout that comprehensively minimizes parasitic capacitances.

Keywords: *Electric Motorcycle Charger; LLC Resonant Converter; Parasitic Capacitances; Planar Transformers; Winding Layout Optimization.*

1. Introduction

The demand for high power density in electric vehicle (EV) applications has led to the adoption of higher operating frequencies, reducing component size [1]. However, this also increases switching losses [2] and electromagnetic interference (EMI) [3], which can degrade efficiency. Soft-switching techniques, such as LLC resonant converters, help mitigate switching losses and allow for high-frequency operation [4]. LLC converters offer a cost-effective solution with consistent soft-switching across a wide power range. Planar transformers with PCB windings are preferred in LLC converters due to their ability to reduce skin effect losses, providing compact, high-frequency solutions [5]-[6]. However, planar transformers face challenges, including a larger footprint, lower copper fill factor, and limited winding capability.

A key limitation in planar transformers, especially for high-frequency applications, is the high parasitic capacitance from the close stacking and large surface area of PCB windings [5]-[6]. As shown in 1, these parasitic capacitances—primarily intra-winding and inter-winding capacitances—affect LLC resonant converter performance. Intra-winding capacitance is the capacitive coupling between turns within the same winding, while inter-winding capacitance results from coupling between separate windings, especially in interleaved designs, which alternate primary and secondary windings to reduce leakage inductance and AC winding losses.

Parasitic capacitances in LLC converters introduce operational challenges such as waveform distortion, increased conduction losses, and voltage irregularities. These capacitances cause high-frequency oscillations and ”ringing” in current and voltage waveforms, leading to higher RMS current through transformer windings and switching devices, which raises conduction losses and reduces efficiency. Voltage distortions, like overshoots and undershoots, can exceed safe limits, impairing voltage regulation and potentially damaging sensitive loads [7]-[9]. At light loads, parasitic capacitances worsen these issues by causing unpredictable voltage gain and erratic behavior, threatening system stability [10]-[11]. Additionally, they interfere with soft-switching by increasing the current needed for zero-voltage switching (ZVS), which can lead to higher conduction losses, partial hard-switching, and increased EMI [12]-[14]. Inter-winding capacitance also contributes to common-mode noise, inducing currents that disrupt converter operation and affect nearby devices [15]-[16], [23]. Therefore, minimizing parasitic capacitances is essential for improving efficiency, voltage regulation, and EMI compliance.

Several strategies have been proposed to reduce parasitic capacitances in planar transformers. The non-overlapping winding method reduces both intra- and inter-winding capacitances by minimizing overlap and increasing the distance between layers, but it significantly increases DC resistance, leading to higher conduction losses [7]. The Zero Voltage Gradient method is effective in reducing intra-winding capacitance and can be combined with an air-gap to reduce inter-winding capacitance [7], all without increasing DC resistance. However, ZVG does not completely eliminate common-mode (CM) current and may still require additional efforts to mitigate the CM noise generated by planar transformers. The ZCC method groups wires into paired and non-paired layers to eliminate common-mode (CM) current by minimizing voltage potential differences [19]. However, it does not implement specific measures to reduce intra-winding capacitance, which remains high due to the substantial voltage gradients between non-paired and paired layers, significantly contributing to the overall parasitic capacitance.

Despite these current methods can reduce both intra-winding and inter-winding capacitance, but they cannot fully

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eliminate both common-mode (CM) current and achieve low overall capacitance, without increasing DC resistance. This research proposes a comprehensive mitigation method that eliminates common-mode current, reduces both intra- and inter-winding capacitance, and maintains low resistance.

The paper is organized as follows: Section 2 calculates parasitic capacitances using the energy conservation method. Section 3 analyzes the Zero Common-Mode Current (ZCC) approach and proposes a new method to reduce parasitic capacitances. Section 4 evaluates the proposed method. Section 5 presents experimental results to validate the proposed method, and Section 6 concludes with key findings and implications for planar transformer design.

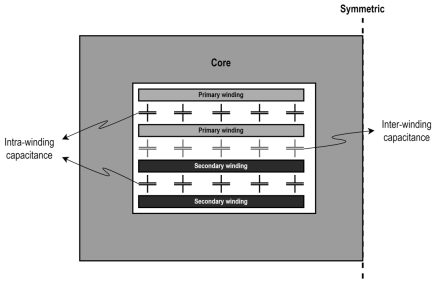


Figure 1: Two concepts of parasitic capacitances.

2. Calculation method for electrostatic energy storage

2.1 Energy storage between two layers

In planar transformers, static capacitance is determined by evaluating the capacitance between consecutive layers. This capacitance represents the charge accumulation between two equipotential surfaces, where each layer is shorted to calculate the capacitance between them. The static capacitance depends on the geometric characteristics of the layers and can be expressed as:

$$C_0 = \varepsilon_0 \varepsilon_r \frac{A_t}{d} \tag{1}$$

where A_t is the overlapping area between the layers, d is the separation distance, and ε_0 and ε_r are the permittivity of free space and the relative permittivity of the material between the layers, respectively. Due to the uneven voltage distribution across the layers, the static capacitance does not charge uniformly. As a result, the equivalent parasitic capacitance is typically calculated by evaluating the electrostatic energy stored between two consecutive layers.

Considering two one-turn layers as illustrated in Fig. 2, the top layer has terminals A and B, while the bottom layer has terminals C and D. The x-axis is defined along the length of the turns, and the y-axis along the width. The stored electrostatic energy between the two layers can be calculated using:

$$E_{ll} \approx \frac{1}{2} \int_0^L \int_0^W C_0(x,y) \Delta V^2(x,y)\, \mathrm{d}y\, \mathrm{d}x \tag{2}$$

where $C_0(x,y)$ is is the local static capacitance at position (x,y) and $\Delta V(x,y)$ is the local voltage difference at position (x,y). By applying Equation 1 to this expression within the energy formulation, the stored electrostatic energy can be rewritten as:

$$E_{ll} \approx \frac{\varepsilon_0 \varepsilon_r}{2d} \int_0^L \int_0^W \Delta V^2(x,y)\, \mathrm{d}y\, \mathrm{d}x \tag{3}$$

The voltage difference $\Delta V(x,y)$ voltage difference is expressed as:

$$\Delta V(x,y) = V_{BD} + V_{AB}(x,y) - V_{CD}(x,y) \tag{4}$$

where V_{BD} represents the voltage difference between Terminal B and Terminal D, corresponding to the overall potential difference between the two layers. The term $V_{AB}(x,y)$ denotes the voltage difference between a point located at position (x,y) on the upper layer and Terminal B, describing the distributed voltage along the winding in the upper layer relative to Terminal B. Similarly, $V_{CD}(x,y)$ represents the voltage difference between a point at position (x,y) on the lower layer and Terminal D, describing the distributed voltage along the winding in the lower layer relative to Terminal D.

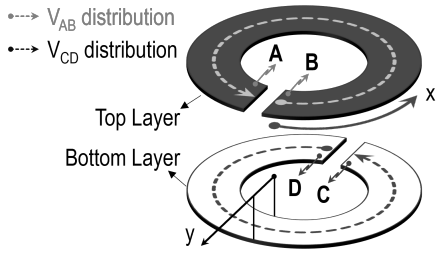
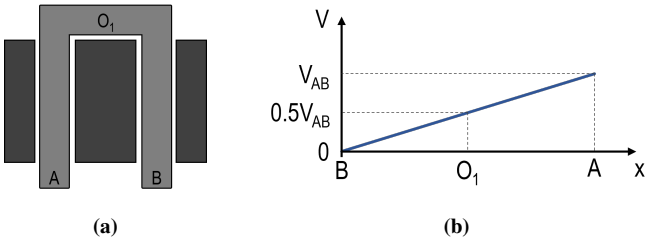


Figure 2: Illustration of two PCB layers.

2.2 Voltage distribution of two layers

This section discusses the voltage distribution of two layers of the E-core transformer. To analyze the voltage distributions in this transformer, a single turn is examined. As shown in Fig. 3a, the turn is divided into two half-turns: one between terminal A and O, and the other between terminal O and B. These half-turns are positioned inside the E-core, resulting in equal magnetizing inductances and induced voltage differences [17]. Assuming a linear voltage distribution along the turn, the voltage profile for one turn in an E-core is illustrated in Fig. 3b.



(a) (b)

Figure 3: Voltage distribution along one turn in E-core based transformer

The findings on voltage distribution can be extended to calculate the voltage difference between two layers in a transformer. These layers can belong to the same winding or different windings. For two one-turn layers in the same winding, as illustrated in Fig.4a, the layers are identical in

direction. The first layer (with terminals A and B) and the second layer (with terminals C and D) have the same voltage difference, i.e., $V_{AB} = V_{CD}$.

As shown in Fig. 4b, the voltage difference between two layers along the x-axis is consistent. Therefore, at any point, the voltage difference can be expressed as: $\Delta V(x,y) = V_{BD}$. The stored energy between two one-turn layers is then derived from Equation 2 and expressed as:

$$E_{ll,\text{intra}} \approx \frac{C_0 \times V_\Delta^2}{2} \tag{5}$$

where $V_\Delta = V_{BD}$.

For two one-turn layers in different windings, as illustrated in Fig. 5a, one layer is rotated 180°, a common configuration in winding layouts. The first layer, with terminals A, B, and midpoint O_1, and the second layer, with terminals C, D, and midpoint O_2, have voltage distributions shown in Fig. 5b.

Due to interruptions at terminals C and D along the x-axis, the voltage distribution is divided into two uniform parts. Here, the voltage of one turn is defined as $V_{\text{turn}} = V_{CD}$, and the voltage difference between the two turns is $V_\Delta = V_{BD}$. The energy E_{inter} stored between two one-turn layers in different windings can be calculated using the voltage differences and is expressed as follows:

$$E_{\text{ll, inter}} = \frac{C_0}{2} \times \left(V_\Delta^2 + \frac{V_{\text{turn}}^2}{4} \right) \tag{6}$$

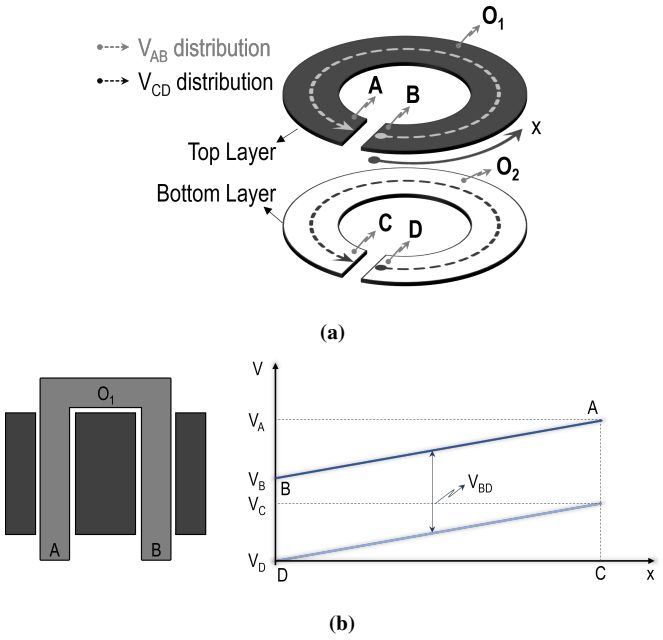


Figure 4: a) Layout of the same winding, and b) voltage difference between them.

The energy storage between any two one-turn layers can be calculated using equations (5)–(6). To apply these equations to a planar transformer, the voltage potentials of each turn must first be determined. For a planar transformer with N_p primary turns and N_s secondary turns, as illustrated in Fig. 6, the transformer is modeled as a three-port system. The three distinct voltages are V_p, the primary voltage; V_s, the secondary voltage; and V_o, the voltage difference between the two windings.

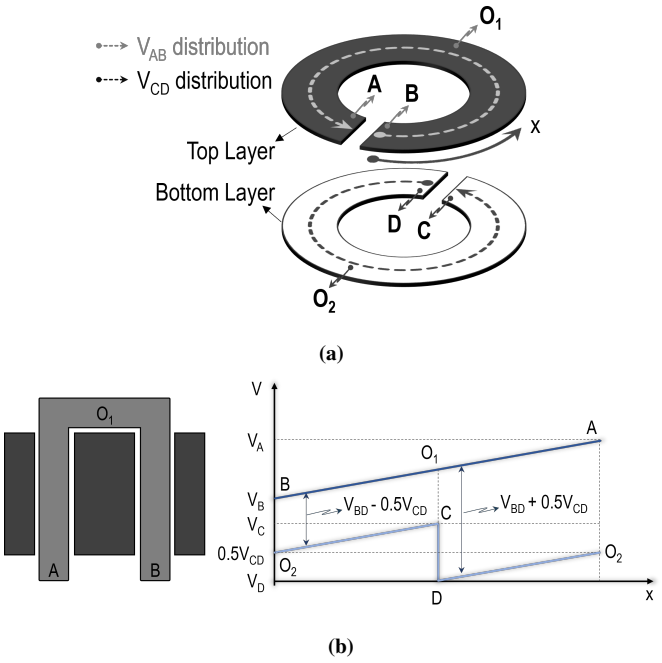


Figure 5: a) Layout of the different winding, and b) voltage difference between them.

Assuming the conventional turns ratio relationship $\frac{V_p}{V_s} = \frac{N_p}{N_s}$, the voltage of each turn is expressed as:

$$V_{\text{turn}} = \frac{V_p}{N_p} = \frac{V_s}{N_s} \tag{7}$$

The voltage difference between two primary turns n_1^{th} and n_2^{th} is:

$$V_\Delta = (n_2 - n_1)V_{\text{turn}} \tag{8}$$

Similarly, the voltage difference between two secondary turns m_1^{th} and m_2^{th} is:

$$V_\Delta = (m_2 - m_1)V_{\text{turn}} \tag{9}$$

Finally, the voltage difference between a primary turn n^{th} and a secondary turn m^{th} is given by:

$$V_\Delta = (n - m)V_{\text{turn}} - V_o \tag{10}$$

To summarize, the storage energy between two one-turn layers can be extracted using equations (5)–(10). The energy storage formulas for two multi-turn layers can be easily derived from equations (5)–(6) by dividing the layers into multiple one-turn layers. The total storage energy of a planar transformer can be

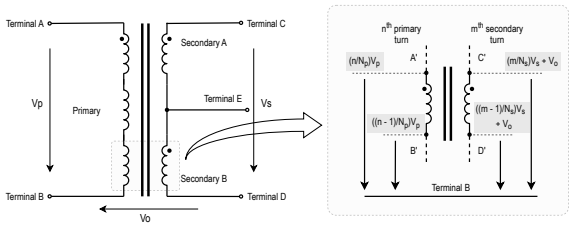


Figure 6: The voltage of the turns in a transformer with three distinct voltages V_p, V_s, and V_o applied to transformer terminals.

calculated by summing the energy stored between each pair of adjacent layers, as expressed by the following equation:

$$E_{\text{total}} = \sum_{i=2}^{k} E_{\text{ll},i-1,i} \tag{11}$$

where i is the index of the layer, k is the total number of layers, and $E_{\text{ell},i-1,i}$ is the storage energy between the $(i-1)$-th and i-th layers.

3. An improved winding layout

Inter-winding capacitance (C_{inter}) creates a path for common mode (CM) current, leading to EMI. Two common solutions are the shielding method and the ZCC method. Shielding, though effective, reduces system efficiency due to low PCB utilization and eddy current losses. The ZCC method, however, fully utilizes PCB space and is more efficient. While conventional ZCC reduces CM current, it doesn't address intra-winding capacitance, which can lead to high total capacitance. This section analyzes the ZCC method and proposes an enhanced solution by combining it with intra-winding capacitance reduction.

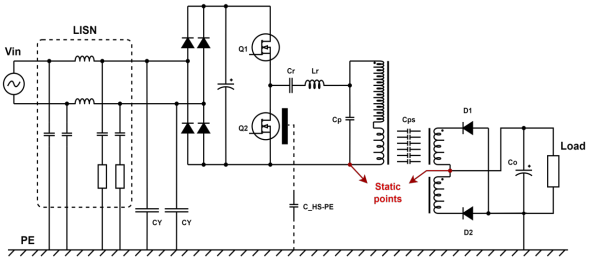


Figure 7: Secondary ground is connected to PE for the safety purpose.

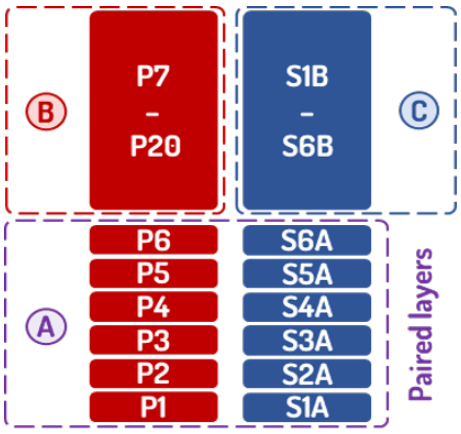


Figure 8: Divide the layers into three group: A. The primary-secondary paired layers, B. The primary non-paired layers, C. The secondary non-paired layers.

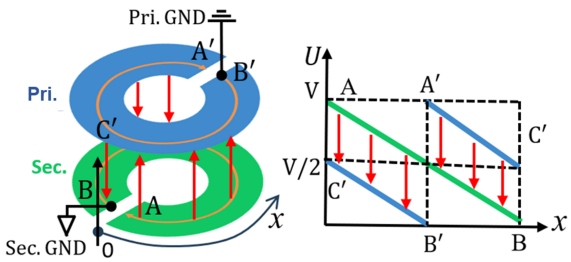


Figure 9: Voltage fluctuation distribution of two paired layers in the planar transformer.

3.1 Analysis the conventional ZCC method

3.1.1 *Voltage fluctuation dV/dt of each turn determination*

The ZCC method is based on voltage distribution, requiring the determination of voltage fluctuation $\frac{dV}{dt}$ across each transformer turn. Considering the LLC configuration in Fig. 7, the primary side uses a half-bridge topology, and the secondary side uses a center-tap topology. According to [20], the secondary ground is typically connected to power earth (PE) for safety, making both the primary and secondary grounds static points. Additionally, the primary terminal connected to the primary ground and the middle terminal of the secondary winding are also static points. In total, two static points are created in the transformer.

These static points serve as references for determining the voltage fluctuation $\frac{dV}{dt}$ of the transformer turns. The following three rules apply:

1. Voltages at the static points are constant and have no $\frac{dV}{dt}$.
2. The voltage increment ΔV after each turn is equal to $\frac{\Delta V_P}{N_P}$, where ΔV_P is the primary voltage fluctuation and N_P is the number of primary turns.
3. Dot points experience the highest $\frac{dV}{dt}$, while non-dot points experience the lowest.

Consider a 20:6:6 turn ratio transformer, as shown in Fig. 7. The primary winding consists of 20 turns, from P1 to P20, with P1 connected to the primary ground, making it a static point. P20 is connected to the dot point of the primary winding. The secondary winding is split into two halves: secondary A (6 turns from S1A to S6A) and secondary B (6 turns from S1B to S6B). S1A and S6B are connected to the secondary static point, S6A is connected to the dot point of secondary winding A, and S1B is connected to the non-dot point of secondary winding B. Based on the three rules and the two static points, P1 is paired with S1A, P2 with S2A, and so on, forming six pairs of layers.

The winding layers can be divided into three groups as shown in Fig. 8. The first group consists of paired primary and secondary layers with the same $\frac{dV}{dt}$. The second group includes the remaining primary layers, and the third group contains the remaining secondary layers.

3.1.2 *Analysis of CM current between two paired layers*

Considering two paired layers illustrated in Fig. 9, they are overlapped with a 180° rotation, which is a common layout for a planar transformer. The difference between the voltage fluctuations of the two layers is divided into two segments. Let the primary voltage be V_{pri} and the secondary voltage be V_{sec}. Along the first half turn, the voltage difference is $V_{\text{pri}} - V_{\text{sec}} = \frac{-V}{2}$, while along the second half turn, the voltage difference is $V_{\text{pri}} - V_{\text{sec}} = \frac{V}{2}$. These two segments have the same voltage difference magnitude but opposite signs. Furthermore, the segments have the same length L, and according to the CM current model expressed in Equation (13), this leads to two equal amounts of CM current in opposite directions from the primary layer to the secondary layer. Consequently, the total generated CM current is zero.

$$i_{\text{CM}} = \int_0^L C_{\text{ps}}(x)\left(\frac{dV_{\text{pri}}}{dt} - \frac{dV_{\text{sec}}}{dt}\right)dx \tag{12}$$

where $C_{\text{ps}}(x)$ is the inter-winding capacitance at position x along the length of the layer, and L is the length of each layer.

The ZCC winding layout eliminates CM current by ensuring only paired layers overlap, as shown in Fig. 13. This design fully utilizes the PCB area, reducing conduction losses, but does not affect intra-winding capacitances.

However, non-paired primary layers exhibit higher voltage potentials, causing significant voltage gradients in overlapping regions, which increases parasitic capacitance. Without methods to reduce intra-winding capacitance, it remains high, significantly contributing to overall parasitic capacitance, as seen in Table 1.

3.2 Proposed method

3.2.1 Introduce the idea concept

To reduce high intra-winding capacitances, two main approaches can be applied: increasing the distance between overlapping layers or inserting air gap layers between them. Fig. 10 shows a 4-layer PCB stack-up, where the prepreg thickness is 0.17 mm and the core thickness is 0.96 mm. Paired layers, due to their identical dV/dt, are effectively placed on opposite sides of the prepreg layer, avoiding increased parasitic capacitance. The remaining primary and secondary layers can be placed on the remaining two layers of the PCB. The substantial thickness of the core layer also contributes to reducing parasitic capacitances. Furthermore, introducing an air gap between successive PCBs can further minimize these capacitances. Despite these improvements, primary layers without secondary pairs still contribute to energy storage, which can be further reduced using alternating or zero-voltage-gradient layouts.

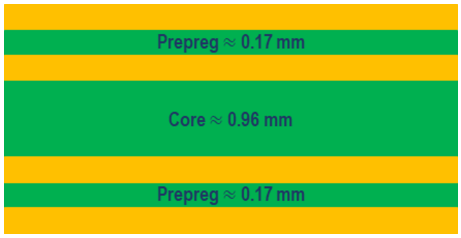


Figure 10: The stack-up of the 4-layer PCB.

3.2.2 Propose the improved Zero common-mode current winding layout

The 48V/3A transformer with a 20:6:6 turn ratio, used in the E-bike charger application, is employed to implement the proposed method. The procedure includes nine steps, which are presented in the flowchart shown in Fig. 11.

The final winding layout of the 20:6:6 transformer is shown in Fig. 13c. Due to the project's limitation of 6 PCBs, PCBs 3 and 4 did not adopt the improved method. These PCBs separate non-paired and paired layers with 0.17 mm thick prepreg, resulting in large parasitic capacitances due to high voltage differences between layers. However, PCBs 1, 2, 5, and 6 use the improved method to reduce intra-winding capacitance. For instance, in PCB1, layers P17-P16 and P6 are separated by 0.96 mm thick FR4 core, minimizing parasitic capacitance despite the large voltage difference. In conclusion, the proposed layout significantly reduces overall parasitic capacitances, as shown in the results in the following sections.

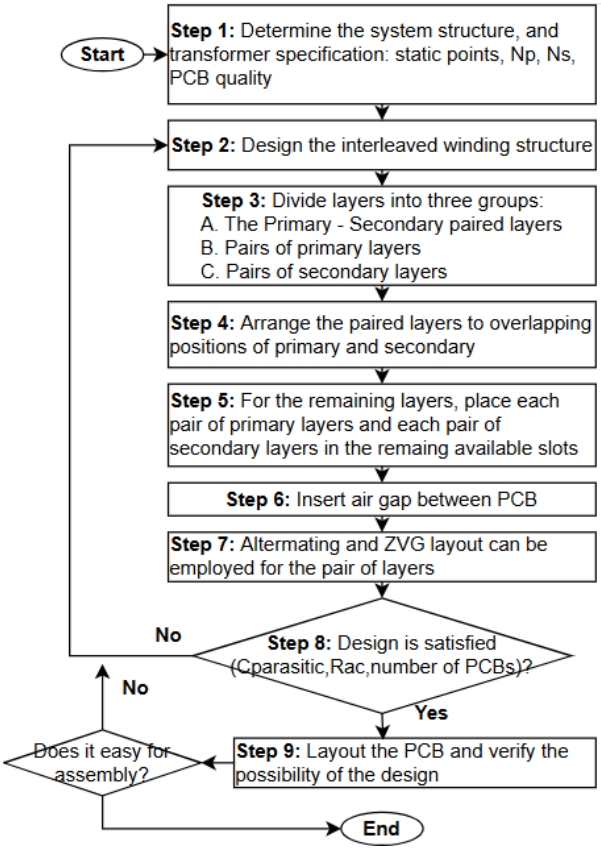


Figure 11: Design procedure of the proposed method.

4. Evaluation the proposed transformer

4.1 Two parameters stray capacitance and equivalent mutual capacitance

In the following subsection, stray capacitance (C_{stray}) and equivalent mutual capacitance (C_{eq}) are introduced to analyze the impact of parasitic capacitances, as shown in Fig. 12. C_{stray} represents the capacitance across the primary winding, calculated from the energy stored in the transformer (11), and serves as an indicator of overall capacitance. C_{eq} represents the inter-winding capacitance responsible for displacement currents between the primary and secondary windings, derived from the common-mode current (12). To minimize CM current, C_{eq} should approach zero. In summary, both C_{stray} and C_{eq} should be minimized to reduce the effects of parasitic capacitances on transformer performance.

$$E_{\text{total}} = \frac{C_{\text{stray}} \times V_{\text{pri}}^2}{2} \tag{13}$$

$$i_{\text{CM}} = C_{\text{eq}} \times \frac{dV_{\text{pri}}}{dt} \tag{14}$$

4.2 Comparison of three transformer winding layouts

In this subsection, three transformer winding layouts, shown in Fig. 13, are compared based on calculations and simulations using the 2D FEA software FEMM 4.0. Fig. 13a represents the traditional transformer winding layout, which follows a conventional interleaved winding arrangement without employing any specific technique to minimize parasitic capacitances or common-mode (CM) current. Fig. 13b

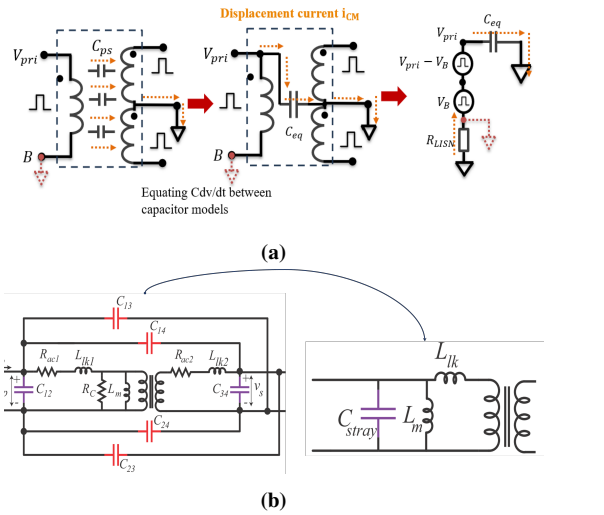


Figure 12: Two parameters (a) stray capacitance, and (b) equivalent mutual capacitance used for parasitic capacitance evaluation.

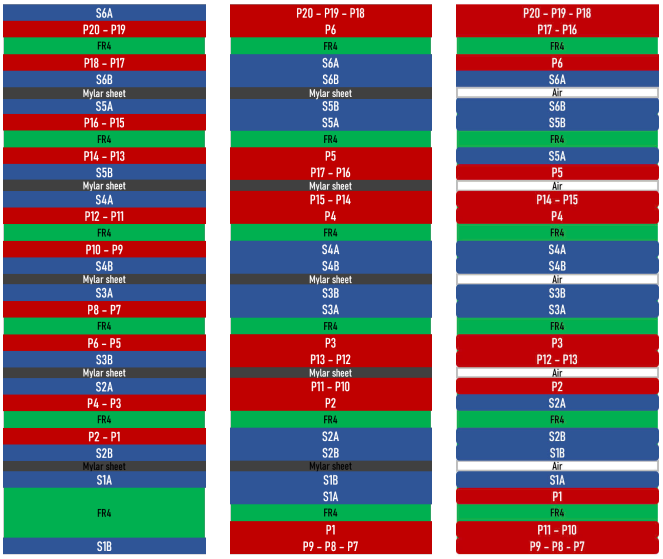


Figure 13: The winding layouts of three transformers with: (a) traditional, (b) conventional ZCC, and (c) proposed method. A layer of Mylar sheet 0.15 mm thick is inserted between two successive PCBs in traditional and ZCC transformers. The air gaps used in proposed transformer also have 0.15 mm thick.

illustrates the Zero Common-Mode Current (ZCC) winding layout in its standard form, where paired layers are arranged to cancel CM current. However, this design does not incorporate additional methods to reduce intra-winding capacitance, which remains relatively high due to significant voltage gradients. Fig. 13c illustrates the transformer winding layout that applies the proposed method, which cancels CM current and reduces intra-winding capacitance through optimized layer placement. The comparison covers three aspects: stray capacitance, equivalent mutual capacitance, and resistances.

Firstly, the stray capacitance analysis shows the electric field density for the three transformer designs (traditional, ZCC, and proposed) in Fig. 14. A 1V voltage is applied to the primary windings, with the secondary windings spanning -0.6V to 0.6V due to the 20:6:6 turn ratio. The electric field density decreases from the traditional transformer to the ZCC and proposed transformers, indicating reduced parasitic capacitance. Table 1 presents a comparison of key parameters for the three transformers, including stray capacitance , equivalent mutual capacitance , DC resistance , and AC resistance .

Table 1: Comparison of Stray Capacitance, Equivalent Mutual Capacitance, and Resistance for Three Transformer Designs

	C_{inter}	C_{eq}	R_{dc}	R_{ac}
Traditional transformer	443 pF	529 pF	90.3 mΩ	95.7 mΩ
ZCC transformer	229 pF	0 pF	90.3 mΩ	108 mΩ
Proposed transformer	115 pF	0 pF	90.3 mΩ	108 mΩ

Firstly, regarding stray capacitance, the ZCC transformer achieves a 50% reduction compared to the traditional design. The proposed transformer further reduces stray capacitance by a factor of four compared to the traditional design and twofold compared to the ZCC transformer by optimizing the winding layout with FR4 cores and air gaps.

Secondly, the comparison of common-mode (CM) current among the three transformers is presented. The traditional transformer exhibits high mutual capacitance, leading to higher CM currents. In contrast, both the ZCC and proposed transformers maintain zero equivalent mutual capacitance, ensuring effective CM current cancellation and significantly reducing CM noise due to the paired layer arrangement.

Finally, the comparison of resistance among the three transformers is now discussed. As shown in Fig. 15, the peak current density simulation results indicate that the traditional transformer exhibits a slightly lower peak current density due to its densely interleaved structure. This structural arrangement helps reduce local current concentration, but it does not significantly impact overall resistance. The resistance results, presented in Table 1, reveal that all three transformers have the same DC resistance. However, the proposed transformer exhibits only a 13% higher AC resistance than the traditional transformer, maintaining high efficiency.

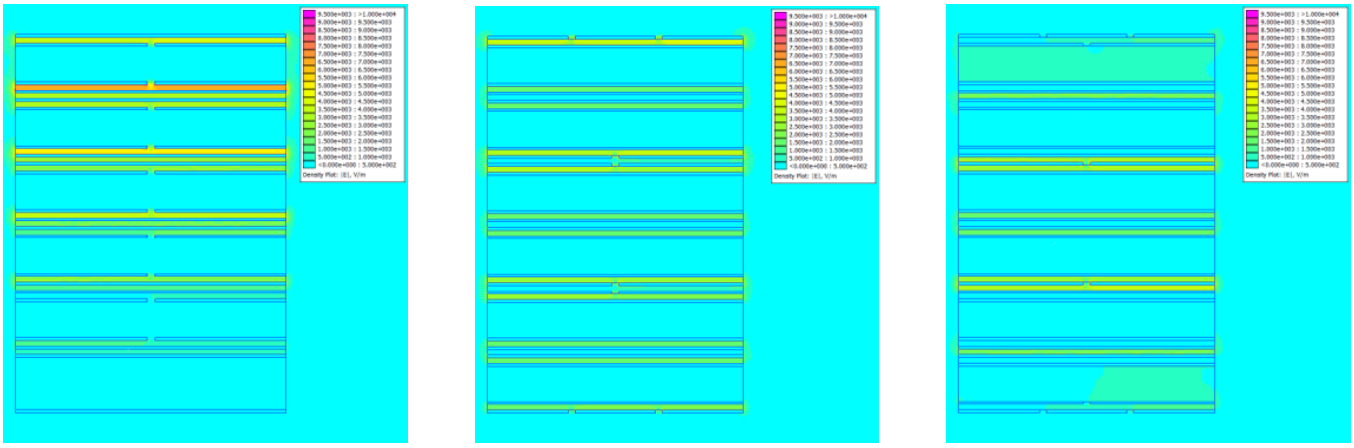
5. Experimental results

In this section, two transformer prototypes shown in Fig. 16 are built to verify the design method. A 180 W LLC converter is developed for E-bike charger application. The two prototypes are tested in the same experimental setup for a fair comparison, and the testing conditions are listed in Table 2.

Table 2: Testing conditions of the system

Test Condition	**Value**
Input Voltage (V)	230 Vrms
Output Voltage (V)	32 Vdc - 58 Vdc
Output Current (A)	3 A
Source	Programmable AC Source
Load	Battery Simulator

The impedance of both transformers can be measured indirectly using the Rigol DSA815 spectrum analyzer, with the setup shown in Fig. 17. According to [21], the frequency at the minimum peak corresponds to the resonant frequency between L_m and C_{stray}. Therefore, C_{stray} for both transformers can be



(a) Traditional Transformer - $E_{total} = 251pJ$ **(b)** ZCC Transformer - $E_{total} = 113pJ$ **(c)** Proposed Transformer - $E_{total} = 60pJ$

Figure 14: Electric field density of three transformer winding layouts. A 1 V are applied to primary windings of all transformer. Considering the static points, 0 V is the voltage of the middle terminal of the secondary winding. The turn ratio is 20:6:6, so secondary winding are applied voltage range from -0.3 V to 0.3 V. E_{total} is the total energy storage in the transformer.

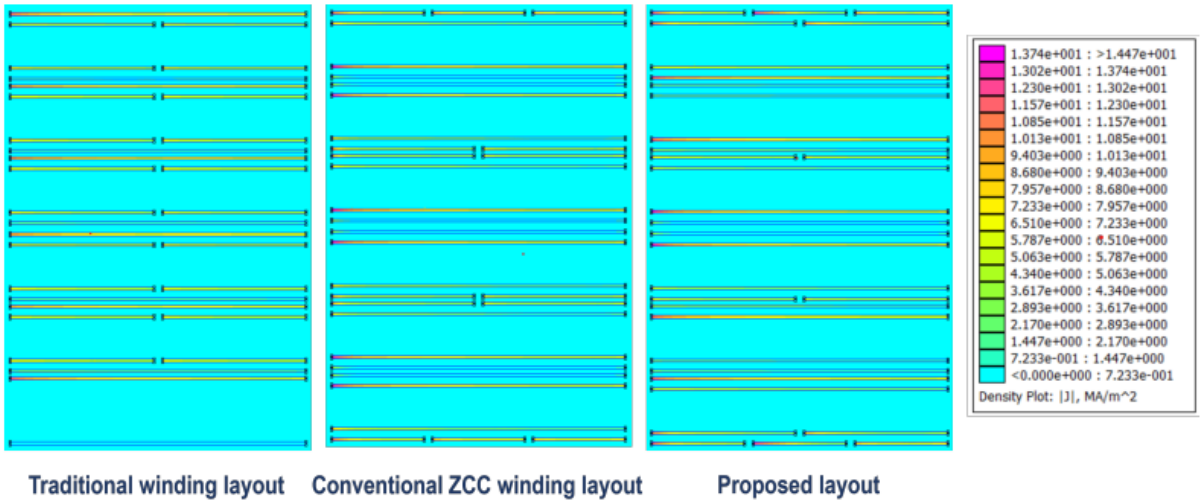
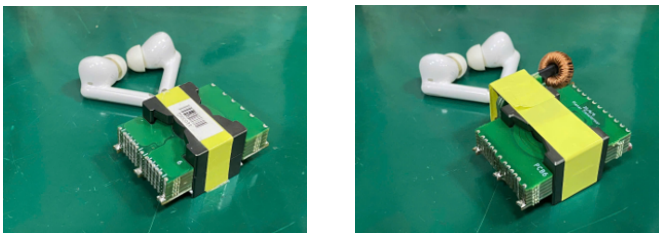


Figure 15: Peak current density of three transformers. The rated sinusoidal current is applied for all windings.



(a) **(b)**

Figure 16: Two transformer prototypes: (a) traditional transformer, and (b) proposed transformer.

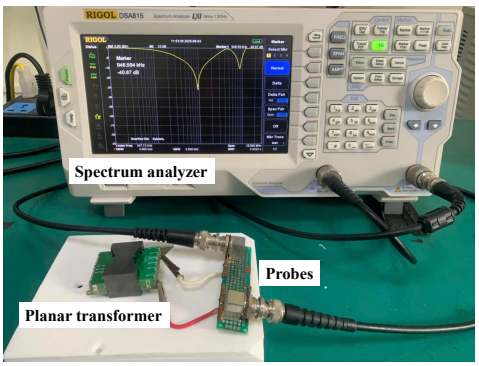


Figure 17: Impedance measurement setup.

extracted from the experimental results shown in Fig. 18.Next, the C_{stray} value was extracted from the simulation results in Section 4.2, while the calculated C_{stray} value was determined based on the method presented in Section II. The experimental, simulation, and theoretical results are compared in Table 3.

The calculated value is lower than the simulated value because the adjacent layer energy is neglected in the calculation method. Meanwhile, the experimental result is lower than the calculated value due to inaccuracies in PCB dimensions and the dielectric constant between layers, which are difficult to control precisely. However, the deviation between calculation and experiment remains below 10%, demonstrating that the proposed calculation method is highly accurate and can be used to estimate parasitic capacitance in practical designs. Notably, the overall parasitic capacitance of the proposed transformer is 75% lower than that of the traditional transformer, highlighting

the effectiveness of the proposed method in achieving the goal of parasitic capacitance reduction.

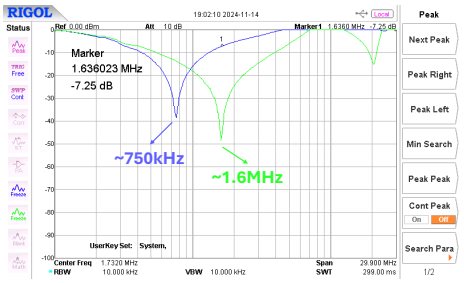
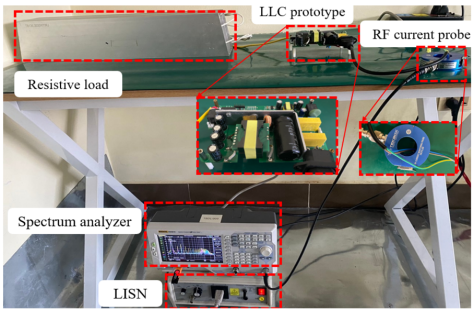


Figure 18: Impedance measurement result.

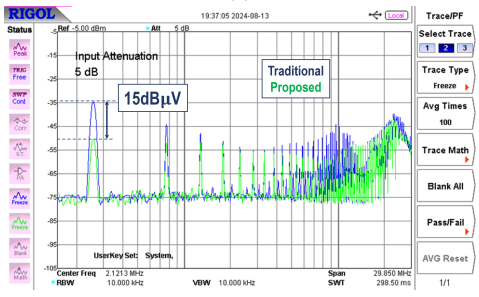
Table 3: Overall parasitic capacitance of traditional transformer and proposed transformer.

	C_{stray}		
	Calculation	Simulation	Experiment
Traditional transformer	443 pF	502 pF	417 pF
Proposed transformer	115 pF	112 pF	105 pF

To verify the CM noise reduction of the proposed transformer, the testing setup shown in Fig. 19a is used. The system is connected to an AC LISN (TBLC08), and CM noise is measured using an RF current probe (TBCP2-250), which cancels differential mode currents by passing both input wires through the probe. The results in Fig. 19b show that the proposed transformer achieves a significant CM noise reduction, with up to 15 dBμV less noise compared to the traditional transformer.



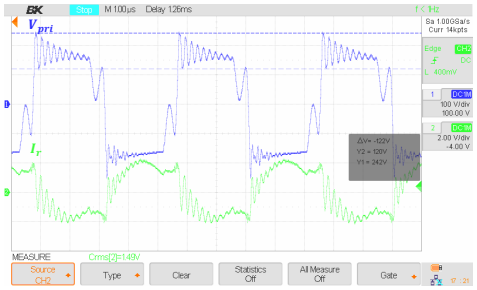
(a)



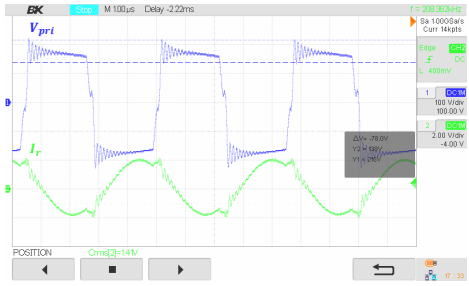
(b)

Figure 19: The CM noise test: (a) setup, and (b) result.

Figure 20 presents the experimental waveforms comparing the traditional transformer and the proposed transformer, illustrating the differences in primary winding voltage and resonant current. In these waveforms, V_{pri} represents the primary winding voltage, while I_r denotes the resonant current in the LLC converter. The results indicate that the proposed transformer exhibits significantly lower voltage spikes compared to the traditional transformer, demonstrating the advantage of reduced stray capacitance. The reduction in voltage spikes alleviates the stress on switching devices, potentially allowing the use of components with lower voltage ratings, thereby reducing overall system costs. Furthermore, the reduced stray capacitance minimizes the oscillation in resonant current, which may lead to lower RMS current and improved efficiency in converter operation.



(a)



(b)

Figure 20: The waveform test: (a) traditional transformer, and (b) proposed transformer.

The system efficiency was evaluated over the entire output voltage range using the Power Analyzer GPM 8310. As shown in Fig. 21, the efficiency results account for contributions from the input EMI filter, relay, auxiliary power supply, and other circuit elements. The data indicate that the system using the proposed transformer configuration achieves slightly higher efficiency than the traditional transformer, with any difference likely due to measurement inaccuracies. Importantly, the proposed design maintains system efficiency while effectively minimizing parasitic capacitances, confirming that reducing parasitic effects does not compromise performance. The peak efficiency recorded was 91.59%, highlighting the proposed transformer's potential for achieving both low parasitic capacitances and high efficiency in practical applications.

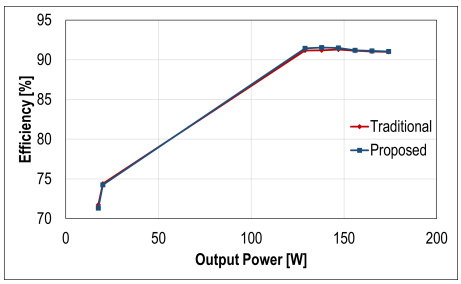


Figure 21: Measured system efficiency over the full output voltage range

6. Conclusion

In conclusion, this paper introduces a new transformer winding layout that successfully mitigates parasitic capacitance impacts. Existing methods, such as non-overlapping layouts and voltage distribution techniques, address some capacitance issues but either increase DC resistance or fail to fully eliminate common-mode (CM) current. The proposed method combines the ZCC approach with intra-winding capacitance reduction techniques, including increasing distances, using air gaps between PCBs, and alternating or ZVG winding layouts. This approach reduces parasitic capacitance by 2 times compared to the ZCC method and 4 times compared to the traditional method, while also eliminating CM current. The system's AC resistance increases by only 13% relative to traditional interleaved layouts, and the proposed transformer reduces CM noise by 15 dBμV without sacrificing system efficiency. The peak efficiency of the system was recorded at 91.59%, confirming that the proposed design maintains high efficiency while effectively reducing parasitic effects. This research demonstrates that the proposed method successfully meets the three key objectives: eliminating common-mode current, achieve low overall parasitic capacitance, and maintaining low resistance. These results highlight the feasibility of the proposed method for practical applications.

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