A single-phase quasi-switched boost H-bridge inverter with power loss reduction capability

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Abstract

This paper proposes a novel single-phase quasi-switched boost H-bridge inverter (qSB-HBI) topology combined with a hybrid pulse-width modulation (HPWM) strategy to enhance power conversion efficiency and minimize the requirement for passive components. By integrating the boost and inverter stages into a single power stage, the proposed topology simultaneously achieves voltage boosting and inversion with fewer components compared to conventional impedance-source inverter (ISI) structures. In traditional PWM-based inverters, the double-line-frequency (2ω) power oscillation causes significant DC-link voltage oscillations, requiring large inductors and capacitors. To overcome this issue, the proposed HPWM method combines pulse-width modulation (PWM) and pulse-amplitude modulation (PAM) techniques, allowing the DC-link voltage to oscillate within a controlled range while maintaining high output voltage quality. This approach effectively reduces switching frequency, switching losses, and the size of passive elements. The proposed configuration is capable of buck-boost operation. Experimental verification on a 1-kW laboratory prototype confirms that the proposed configuration achieves lower losses, smaller DC-link capacitance, and significantly improved output voltage quality.

Keywords*: H-bridge inverter; Pulse amplitude modulation; Hybrid pulse width modulation; Quasi-switched boost; Impedance-source inverter.*

Symbols

Symbols	Units	Description
M		modulation
V_{PN}	V	DC-link voltage
V_S	V	Power switch voltage
$P_{S,cond}$	W	conduction loss on the power switch
I_{RL}	A	output current of load

Abbreviations

PWM	pulse width modulation
ZSI	Z-Source Inverter
HBI	H-Bridge Inverter
NST	non-shoot-through
PAM	pulse-amplitude modulation
HPWM	hybrid pulse-width modulation

1. Introduction

The inverter is one of the most essential functional units in electrical energy conversion systems, particularly in renewable energy applications, electric drives, energy storage systems, and industrial power electronics. Its primary role is to convert direct current (DC) voltage into alternating current (AC) voltage with the frequency, amplitude, and suitable waveform to meet the requirements of the load or the grid. Conventional inverters, such as voltage source inverters (VSIs), offer high efficiency but lack inherent voltage boosting capability. As a result, they often require an additional DC-DC boost stage, which increases the number of components, circuit size, and control complexity. This limitation has driven the development of integrated boost inverter topologies that can perform both voltage boosting and inversion within a single power stage, thereby reducing losses and enhancing overall system reliability.

The Z-Source Inverter (ZSI) configuration, first proposed by Peng in 2003 [1], marked a breakthrough in inverter design with its inherent voltage-boosting capability through the integration of a Z-network consisting of two inductors and two capacitors connected in an X-shape between the DC source and the power stage. This structure allows the insertion of shoot-through states into the switching cycle without damaging the power switches, while significantly enhancing noise immunity and overall system reliability [2]-[4]. Furthermore, to reduce the size and power losses of the passive components in the ZSI, the quasi-Z-Source Inverter (qZSI) was introduced as an improved variant that minimizes component count and simplifies control while maintaining the same voltage boost capability and shoot-through operation [5]-[7]. The qZSI topology quickly became a foundational structure for many integrated inverter variants, such as the three-level qZSI [8], T-type qZSI, and F-type qZSI [9], [10].

Although the ZSI and qZSI offer distinct advantages, they still require two inductors and two capacitors, which limits their integration capability in low-power systems or applications demanding high power density. To overcome this limitation, the Switched Boost Inverter (SBI) was proposed, which utilizes the operating principle of a conventional boost converter combined with shoot-through capability to achieve both voltage boosting and inversion within a single power stage [11]. The SBI employs only one inductor, one diode, one capacitor, and one additional switch, thereby significantly reducing the number of passive components [12]. Building upon the SBI, the quasi-Switched Boost Inverter (qSBI) integrates the advantages of both qZSI and SBI by utilizing a quasi-switched boost network for voltage boosting, while maintaining compatibility with various modulation strategies and multilevel inverter configurations [13]-[15].

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This topology not only simplifies the hardware design but also offers flexibility in configuration and effectively mitigates leakage current, particularly in grid-connected PV applications [16], [17].

In single-phase single-stage inverter topologies, the quasi-Switched Boost H-Bridge Inverter (qSB-HBI) is considered a suitable candidate due to its ability to integrate the boost network directly into the inverter stage with a reduced number of components. However, similar to other single-phase topologies such as the qZSI, the double-line-frequency (2ω) power fluctuation inherently exists, causing voltage oscillations across the DC-link due to continuous energy exchange between the DC and AC sides [18], [19]. If not properly controlled, this voltage ripple directly affects the output voltage quality, increases harmonic distortion, and degrades the overall system efficiency. In conventional PWM modulation techniques, maintaining a high-quality output voltage typically requires large inductance and capacitance values in the qSB network to suppress the 2ω ripple component on the DC-link. However, this leads to increased size and losses, which are undesirable for systems demanding high power density and compact design. Furthermore, due to the inherent shoot-through capability (simultaneous conduction of both semiconductor switches) of the qSB structure, traditional PWM strategies often result in high switching losses and increased voltage stress across the power devices. In [20], a novel pulse-width modulation (PWM) strategy was introduced for the qZS configuration to reduce switching losses while simultaneously minimizing the required capacitance and inductance in the qZS network.

To address the above-mentioned issues, this paper proposes a hybrid pulse-width modulation (HPWM) strategy applied to the qSB-HBI configuration. This modulation technique combines the principles of pulse-width modulation (PWM) and pulse-amplitude modulation (PAM) to achieve the following advantages: 1) Reduce the switching actions of power devices; 2) Minimize switching losses; 3) Decrease the required capacitance and inductance values by allowing the DC-link ripple to vary within a controlled amplitude range; 4) Maintain the quality of the AC output voltage without increasing the size of the output filter. Moreover, the qSB-HBI configuration employing the HPWM strategy not only achieves high conversion efficiency but also aligns with modern design trends emphasizing compactness, cost-effectiveness, and high performance in small- and medium-scale grid-connected PV systems.

2. Configuration 1P-qSB-HBI-HPWM

Figure 1 illustrates the configuration of the proposed single-phase quasi-Switched Boost H-Bridge Inverter (1P-qSB-HBI). The topology consists of a qSB network inserted between the input DC voltage V_{dc} and the H-bridge inverter stage. The qSB network is responsible for boosting or bucking the input voltage, while the H-bridge inverter generates the desired AC output voltage V_o. The qSB network comprises an inductor L_B, a diode D_1, a capacitor C_1, and two power switches S_1 and S_2. Moreover, in the proposed topology, the required capacitance of C_1 in PAM mode is only 5 μF, whereas conventional qZSI designs typically employ capacitors in the range of 1-2 mF, as in [7], [14], and [15]. This corresponds to a reduction of several orders of magnitude in the required capacitance, which directly leads to a significant decrease in the volume, weight, and cost of the DC-link energy-storage components. The H-bridge inverter includes four power switches S_{A1}, S_{A2}, S_{B1} and S_{B2}. The output of the configuration is connected to a load RL through an LC filter consisting of an inductor L_f and a capacitor C_f.

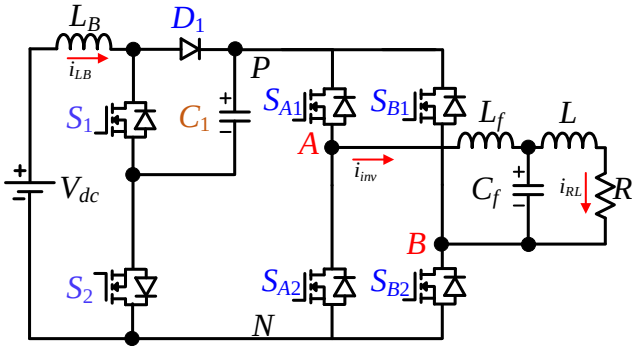

Figure 1: Proposed inverter configuration.

2.1 Operating state

2.1.1 *Boost state*

When the input voltage V_{dc} is smaller than the peak output amplitude $V_{o,peak}$, the proposed inverter operates in boost mode, which includes the shoot-through (ST) state and the non-shoot-through (NST) state (Figure 2).

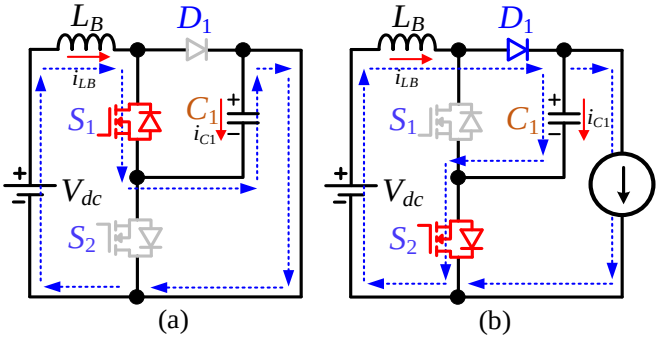

Figure 2: Operation modes of 1P-qSB-HBI. (a) ST state, (b) NST state

ST State (Figure 2(a)): Switch S_1 is ON while S_2 is OFF, and diode D_1 is reverse-biased. In the H-bridge, the two switches in the same leg S_{A1} and S_{A2} or S_{B1} and S_{B2} are simultaneously turned ON. Consequently, the inductor L_B is charged with energy from the input source V_{dc} and capacitor C_1. Capacitor C_1, which discharges through the inductor. The voltage equation across the inductor L_B and capacitor C_1 is determined as follows:

$$\begin{cases} v_{LB} = v_{dc} + v_{C1} \\ i_{C1} = i_{LB} \end{cases} \quad (1)$$

In the non-shoot-through (NST) state, is presented Figure 2(b), the power switch S_1 is turned off, while switch S_2 is turned on, and diode D_1 is forward-biased. At this moment, the inductor L_B discharges its stored energy to the capacitor C_1 and the inverter side. Consequently, capacitor C_1 is charged. The voltage equations across the inductor L_B and the capacitor C_1 can be expressed as follows:

$$\begin{cases} v_{LB} = v_{dc} - v_{C1} \\ i_{C1} = i_{LB} - i_{PN} \end{cases} \quad (2)$$

where i_{PN} is the inverter-side voltage.

In the steady-state condition, the average voltage across the inductor L_B over one switching period T_S is zero. Based on equations (1) and (2), equation (3) can be derived:

$$0 = (V_{dc} + V_{C1}) \cdot DT_S + (V_{dc} - V_{C1}) \cdot (1-D)T_S \quad (3)$$

From formula (3), the output voltage V_{PN} of the qSB circuit in boost mode is determined as follows:

$$V_{PN} = V_{C1} = \frac{V_{dc}}{1-2D} \quad (4)$$

2.1.2 *Buck state*

When the input voltage V_{dc} is greater than the peak amplitude of the output voltage $V_{o,peak}$, the proposed inverter configuration operates in buck mode. In this condition, the quasi-switched boost (qSB) network does not perform any boosting function; the inductor L_B behaves as a conductor, and the capacitor voltage C_1 equals the input voltage V_{dc} (V_{C1} = V_{dc}). By adjusting the modulation index M, the output voltage amplitude can be reduced. The modulation index M is defined as follows:

$$M = \frac{V_{o,peak}}{V_{dc}} \quad (5)$$

In this mode, the power switch S_2 is kept ON continuously, while switch S_1 remains OFF, and diode D_1 is forward-biased. The output voltage of the qSB network, denoted as V_{PN} is determined as follows:

$$V_{PN} = V_{dc} \quad (6)$$

2.2 Control strategy

The Hybrid Pulse-Width Modulation (HPWM) technique, illustrated in Figure 3, is employed to generate the gating signals for the power switches of the proposed inverter. This method combines two modulation strategies: 1) Pulse-Width Modulation (PWM), and 2) Pulse-Amplitude Modulation (PAM). When the peak output voltage $V_{o,peak}$ is lower than the input voltage V_{dc}, the proposed inverter operates in PWM mode. In this case, the circuit functions as a conventional inverter without shoot-through operation. Conversely, when the peak output voltage $V_{o,peak}$ exceeds the input voltage V_{dc}, the proposed inverter operates in PAM mode.

In PWM mode, the proposed inverter configuration does not perform shoot-through operation; therefore, the DC-link voltage is equal to the input voltage V_{dc}. During this period, the proposed inverter operates without any boost action, meaning that only the switches in the H-bridge inverter stage perform switching operations. On the qSB side, the power switch S_1 is turned OFF, while S_2 is turned ON, causing diode D_1 to become forward biased. The capacitor C_1 is charged by the DC input source while simultaneously discharging energy to the inverter side. The output voltage of the proposed configuration in PWM mode is defined as follows:

$$v_o = V_{DC} \cdot M \cdot \sin(\omega t) \quad (7)$$

where M is the modulation index ($0 \le M \le 1$), ω is the angular frequency.

To determine the appropriate operating mode at each instant, an important parameter to identify is the angular position $\omega t = \theta$. At this instant, the output voltage V_o equals the input voltage V_{dc} leading to $M \cdot \sin\theta = 1$. Therefore, the angular position θ is determined as follows:

$$\theta = \arcsin\left(\frac{1}{M}\right) = \arcsin\left(\frac{V_{dc}}{V_{o,peak}}\right) \quad (8)$$

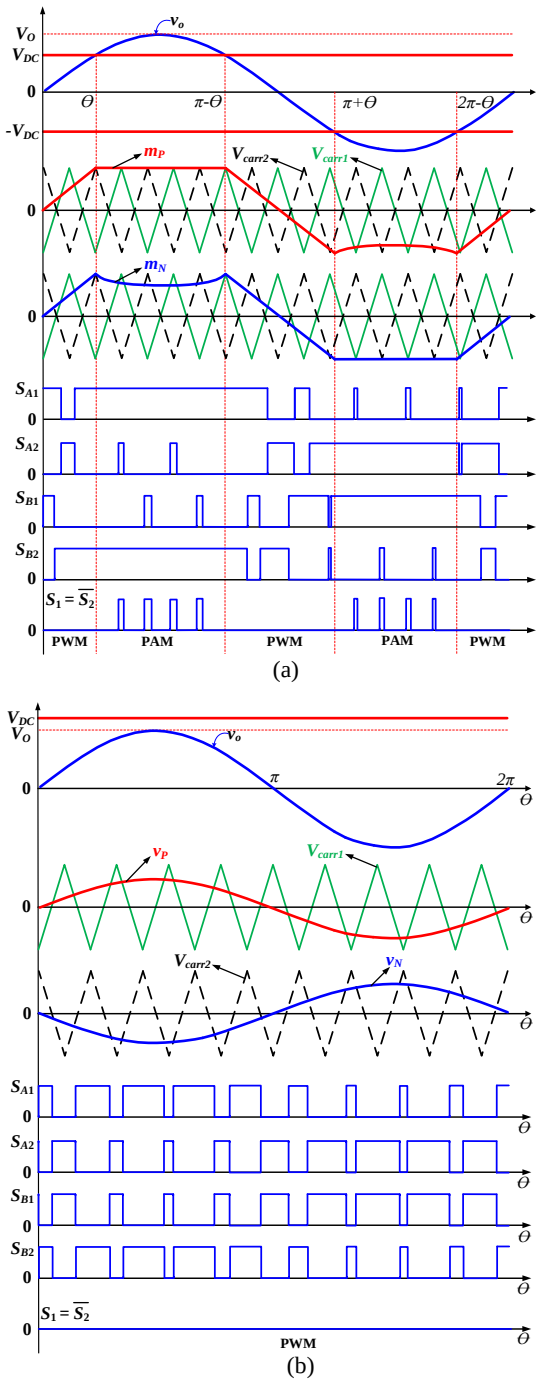

Figure 3: Control algorithm. (a) HPWM mode for boost, (b) PWM mode for buck.

In PAM mode, the output voltage is higher than the DC input voltage; therefore, a boosting operation of V_{PN} is required before the inversion process takes place. During this period, the proposed inverter configuration performs two functions: boosting the DC voltage and converting the DC

voltage into AC voltage. The output voltage of the proposed configuration in PAM mode is defined as follows:

$$v_o = \frac{1}{1-2D} \cdot V_{DC} \cdot M \cdot \sin(\omega t) \tag{9}$$

In the boost mode, the control waveforms shown in Figure 3(a) clearly illustrate the pulse modulation method used to generate the gating signals for the power switches by comparing the modulation signals m_P and m_N with $carrier_1$ and $carrier_2$. The signals m_P and m_N are defined as follows:

$$m_P = \begin{cases} M\sin(\omega t), \omega t \in [0,\ \theta) \cup (\pi-\theta,\ \pi+\theta) \cup (2\pi-\theta,\ 2\pi] \\ \dfrac{\left|M\sin(\omega t)\right|}{1-2\left|M\sin(\omega t)\right|}, \quad \omega t \in [\pi+\theta,\ 2\pi-\theta] \\ 1, \quad \omega t \in [\theta,\ \pi-\theta] \end{cases} \tag{10}$$

$$m_N = \begin{cases} M\sin(\omega t), \omega t \in [0,\ \theta) \cup (\pi-\theta,\ \pi+\theta) \cup (2\pi-\theta,\ 2\pi] \\ \dfrac{-\left|M\sin(\omega t)\right|}{1-2\left|M\sin(\omega t)\right|}, \quad \omega t \in [\pi+\theta,\ \pi-\theta] \\ -1, \quad \omega t \in [\theta,\ 2\pi-\theta] \end{cases} \tag{11}$$

In the buck mode, the gating signals for the power switches are generated by comparing the modulation signals v_P *and* v_N with $carrier_1$ and $carrier_2$. The signals v_P *and* v_N are defined as follows:

$$\begin{cases} v_P = M\sin(\omega t) \\ v_N = M\sin(\omega t + \pi) \end{cases} \tag{12}$$

3. Power loss

The power losses of the qSB-HBI circuit employing the HPWM algorithm include losses in the inductor, capacitor, diode, and power switches. These losses are analyzed in detail as follows.

3.1 Conduction loss

The conduction loss on capacitors C_1, C_2 and inductor L_B is calculated by the formula:

$$\begin{cases} P_{LB} = r_{LB} I_{LB,RMS}^2 \\ P_{Cj} = r_{ESR} I_{Cj,RMS}^2;\ j = 1,2 \end{cases} \tag{13}$$

where r_{ESR} is the internal resistance of the capacitor, r_{LB} is the inductor resistance.

The conduction loss on the diodes and the power switch MOSFET (denoted as $P_{D,cond}$ and $P_{S,cond}$ respectively) is calculated by the formula:

$$\begin{cases} P_{S,cond} = r_{DS,on} I_{S,RMS}^2 \\ P_{D,cond} = V_F I_{D,AVG} \end{cases} \tag{14}$$

where $r_{DS,on}$: MOSFET conduction resistance, V_F: diode forward voltage.

3.2 Switching loss

During the intervals [$\theta \div \pi$-θ] and [π+$\theta \div 2\pi$-θ], the power switch S_1 performs two switching operations (turn-on and turn-off) in each switching period T_s, where the switching current equals the inductor current I_{LB}, and the switching voltage equals the DC-link voltage.

During the intervals [$0 \div \theta$], [π-$\theta \div \pi$+θ] and [2π-θ] the power switch S_1 remains OFF, as illustrated in Figure 3(a). The switching loss of S_1 is determined by the following equation:

$$P_{S_1,sw} = \frac{1}{\pi}\int_{\theta}^{\pi-\theta} 2 \cdot \frac{1}{2} \cdot V_{PN} \cdot I_{LB} \cdot \frac{t_{ri}+t_{fi}+t_{ru}+t_{fu}}{T_S} d\theta \tag{15}$$

where t_{ru}: the voltage rise time during MOSFET turn-off; t_{fu}: the voltage fall time during MOSFET turn-on; t_{ri}: the current rise time during MOSFET turn-on; t_{fi}: the current fall time during MOSFET turn-off.

During the intervals [$\theta \div \pi$-θ] and [π+$\theta \div 2\pi$-θ], the power switch S_2 performs two switching operations in each switching period T_s, where the switching current equals the inductor current I_{PN}-I_{LB}, and the switching voltage equals V_{LB}-V_{dc}. During the intervals [$0 \div \theta$], [π-$\theta \div \pi$+θ], and [2π-θ] the power switch S_2 remains ON, as illustrated in Figure 3(a). The switching loss of S_2 is determined by the following equation:

$$P_{S_2,sw} = \frac{1}{\pi}\int_{\theta}^{\pi-\theta} 2 \cdot \frac{1}{2} \cdot (V_{LB}-V_{dc}) \cdot (I_{PN}-I_{LB}) \cdot \frac{t_{ri}+t_{fi}+t_{ru}+t_{fu}}{T_S} d\theta \tag{16}$$

The diode D_1 performs one switching operation in each switching period T_S with a reverse voltage equal to V_{PN}. The corresponding reverse recovery loss is given by:

$$P_{rr,D_1} = \frac{2}{\pi}\int_{\theta}^{\pi-\theta} 2 \cdot \frac{V_{PN} \cdot Q_{rr}}{T_s} d\theta \tag{17}$$

where Q_{rr} is the reverse recovery charge of the diode.

During the positive half-cycle, within the intervals [$0 \div \theta$] and [π-$\theta \div \pi$], the power switch S_{A1} performs one switching operation per carrier cycle, with the switching voltage is V_{dc} and switching current is I_{RL}, respectively. During the interval [$\theta \div \pi$-θ], switch S_{A1} remains in a steady state with zero switching action. During the negative half-cycle, within the interval [π+$\theta \div 2\pi$-θ], S_{A1} performs one switching operation per carrier cycle, with a switching current of $2I_{LB}$ at a switching voltage of V_{PN}, During the intervals [$\pi \div \pi$+θ] and [2π-$\theta \div 2\pi$], the body diode of switch S_{A1} undergoes reverse recovery, contributing to the total loss. Therefore, the total switching loss of switch S_{A1} is determined by the following equation:

$$\begin{aligned} P_{S_{A1},sw} = \frac{1}{2\pi}\Bigg[& \int_{0}^{\theta} 2 \cdot \frac{1}{2} \cdot V_{dc} \cdot I_{RL} \cdot \frac{t_{ri}+t_{fi}+t_{ru}+t_{fu}}{T_S} d\theta \\ & + \int_{\pi+\theta}^{2\pi-\theta} \frac{1}{2} \cdot V_{PN} \cdot 2I_{LB} \cdot \frac{t_{ri}+t_{fi}+t_{ru}+t_{fu}}{T_S} d\theta \\ & + \int_{\pi}^{\pi+\theta} 2 \cdot V_{PN} \cdot Q_{rr} \cdot f_s d\theta \Bigg] \end{aligned} \tag{18}$$

Table 1: Experimental parameters

Parameters/Equipment		Values
DC Input voltage	V_{dc}	150 V – 400 V
Output frequency	f_0	50 Hz
Switching frequency	f_S	10 kHz
Inductor	L_B, r_{LB}	1 mH/20 A, 0.15-Ω
Capacitor	C_1, r_{ESR}	5uF/ 630 V, 50-mΩ
LC filter	L_f and C_f	1mH and 10 µF
Load resistance	RL	48-Ω, 10mH
Power switches	S_1, S_2, S_{1X} - S_{4X}	MOSFETs C3M0075120K (t_{ru}, t_{fu}: 22 ns and 33 ns; t_{ri}, t_{fi}: 11 ns)
Diode	D_1	60EPF12

The switching losses of power switches S_{A2}, S_{B1} and S_{B2} are determined in the same manner as for S_{A1}. To highlight the efficiency advantage of the proposed inverter, the total power losses of the proposed inverter are compared with a quasi-switched boost inverter [14] and a single-stage qZS-HBI inverter [20]. The parameters used for the topologies [14] and [20] are identical to those of the proposed configuration. This analysis is conducted under operating conditions of an input voltage of 150 V, an output voltage of V_{RMS}, and an output power of 1 kW. The component parameters, including inductors, capacitors, MOSFETs, diodes, and load, are kept the same as listed in Table 1 to ensure a fair comparison.

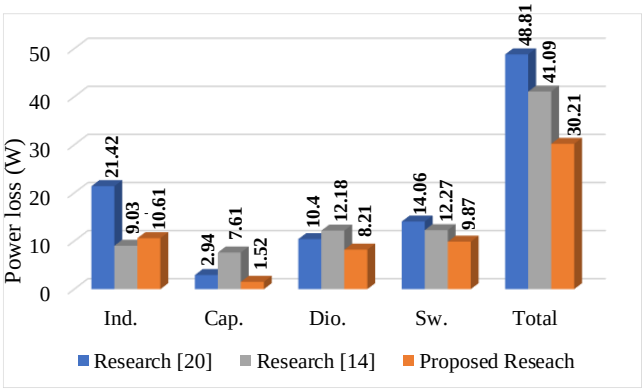

Figure 4: Comparison of power loss of the proposed configuration with the studies [14], [20].

The results shown in Figure 4 indicate that the proposed configuration significantly reduces power losses across most components. For topologies exhibiting similar output-voltage waveforms and comparable device counts. In terms of inductor losses, the topology in [20] exhibits higher inductor loss than both [14] and the proposed topology, because it employs two inductors instead of a single inductor as in [14] and in the proposed topology. For the topology in [14], electrolytic capacitors are used, with a relatively large capacitance and equivalent series resistance ESR (1 mF and 0.15 Ω), whereas both [20] and the proposed converter employ film capacitors with much smaller capacitance and ESR values (5-10 μF and 0.04 Ω). As a result, the capacitor loss in [14] is significantly higher. Although the proposed topology uses one more power switch than [14], the application of the HPWM strategy reduces the total switching loss of the proposed converter by about 2.4 W compared with [14]. Overall, the proposed design achieves the lowest total power loss, 30.21 W, while the total losses of [20] and [14] are 48.81 W and 41.09 W, respectively. This substantial improvement demonstrates the superior advantages of the proposed configuration, not only in terms of power efficiency but also in thermal stress reduction and enhanced operational reliability of the system.

4. Design guidelines

4.1 Selection of passive components

The input current of the proposed configuration is equal to the current flowing through the inductor L_B, as this inductor is directly connected to the DC input source. The average value of the inductor current can be determined by the following expression:

$$I_{LB,AVG} = P_O / (\eta\% \cdot V_{dc}) \tag{19}$$

where P_O is the output power, and η% is the conversion efficiency of the inverter.

The inductor current ripple, denoted as ΔI_{LB}, is calculated using the following equation:

$$\Delta I_{LB} = \frac{2V_{dc}D(1-D)}{(1-2D)L_B f_s} \tag{20}$$

To ensure stable operation, the current ripple ΔI_{LB} must be less than x% of the average current I_{LB}. Therefore, the inductance value L_B should be selected according to the following conditions:

$$L_B \geq \frac{2\eta\%V_{dc}^2(1-D)D}{x\%P_O(1-2D)f_s} \tag{21}$$

where x% is the maximum allowable current ripple across the inductor.

Similarly, the voltage ripple of the capacitor C_1, denoted as ΔV_{C1}, is calculated using the following expression:

$$\Delta V_{C1} = \frac{P_O D T_S}{\eta\% V_{dc} C_1} \tag{22}$$

To ensure the quality of the DC-link voltage, the capacitors C_1 should be selected to satisfy the following conditions:

$$C_1 \geq \frac{P_O D(1-2D)T_S}{y\%\eta\%V_{dc}^2} \tag{23}$$

where y% is the maximum allowable voltage ripple of the capacitors.

4.2 Selection of active components

All the switching switches in the proposed configuration are designed to withstand a maximum voltage stress equal to V_{PN}. The voltage stresses across the power switches (S_1, S_2, S_{A1}, S_{A2}, S_{B1}, S_{B2}) are determined as follows:

$$V_s = V_{PN} = \frac{V_{DC}}{1-2D} \tag{24}$$

The diode D_1 and the power switch S_1 are designed to conduct the current flowing through the inductor L_B. Meanwhile, the power switch S_2 is designed to carry a current equal to (I_{PN}-I_{LB}). The maximum current flowing through these components is determined as follows:

$$\begin{cases} I_{D1,\max} = I_{S1,\max} = I_{LB,\max} = I_{LB} + \dfrac{\Delta I_{LB}}{2} = \dfrac{P_O}{\eta\%V_{dc}} + \dfrac{V_{dc}(1-D)D}{L_B(1-2D)f_s} \\ I_{S2,\max} = I_{PN} - I_{LB} \end{cases} \tag{25}$$

The switches S_{AX} and S_{BX} are responsible for conducting the output current on the inverter side. Therefore, these switches are designed to handle current corresponding to I_{PN}.

5. Experimental results

Figure 5 illustrates the experimental prototype of the single-phase 1P-qSB-HBI inverter controlled by the HPWM technique, with the parameters listed in Table 1. When the DC input voltage is set to 150 V in boost mode and 400 V in buck mode, the inverter generates an AC output voltage of 220 V_{RMS}, meeting the standards of residential power grids. The system employs an FPGA Cyclone II EP2C5T144C8 in coordination with a TMS320F28335 digital signal processor to generate and process the control signals. The output voltage

and current waveforms are measured and recorded directly using an oscilloscope.

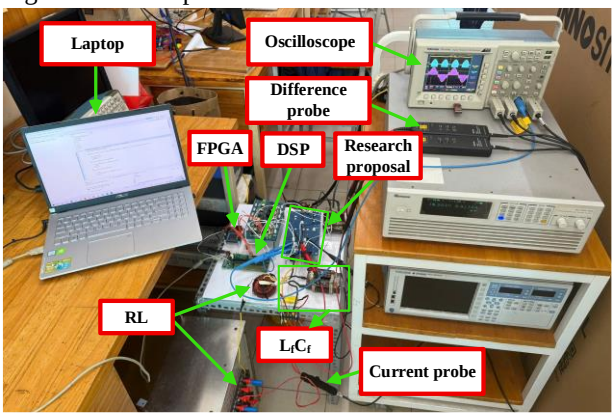

Figure 5: Experimental setup

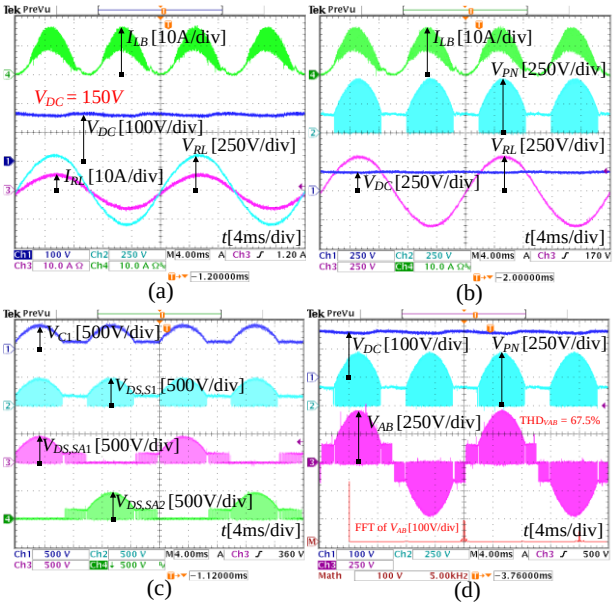

Figure 6: Experimental results with input voltage 150V

The experimental results for the boost mode (with an input voltage V_{dc} =150 V) are shown in Figure 6. The average current through the inductor is 6.15 A. Meanwhile, the RMS values of the output voltage and current (V_{RL} and I_{RL}) are 216 V_{RMS} and 4.22 A_{RMS}, respectively, as illustrated in Figure 6(a). In Figure 6(b), when the instantaneous output voltage is lower than the input voltage of 150 V, the voltage V_{PN} equals the input voltage (V_{PN} =150 V). Conversely, when the instantaneous output voltage exceeds the input voltage V_{dc}, the voltage V_{PN} is boosted through the PAM mode operation, reaching $V_{PN,peak}$=485 V. The voltage stresses across the power switches S_1, S_{A1}, and S_{A2} are equal to $V_{PN,peak}$ = 485 V, as shown in Figure 6(c). The total harmonic distortion of the output voltage V_{AB} (THD_{VAB}) is measured at the inverter output terminals *A* and *B* prior to filtering. When the proposed HPWM method is used in boost operation, the output voltage in the PAM interval has a pulse-amplitude-modulated envelope that follows a sinusoidal reference, as shown in Fig. 6(d). Under this condition, the measured THD of V_{AB} is 67.5%.

With an input voltage of 400 V, the proposed inverter configuration operates in buck mode. The average current through the inductor I_{LB} is 2.32 A. Meanwhile, the RMS values of the output voltage and current are 217 V_{RMS} and 4.22 A_{RMS}, respectively, as shown in Figure 7(a). The voltage V_{PN} remains equal to the input voltage V_{dc} = 400 V, as illustrated in Figure 7(b). In addition, the voltage stresses across the switches are 400 V as presented in Figure 7(c). In the buck operating mode, the waveform of V_{AB} shown in Fig. 7(d) is essentially a two-level waveform, which leads to an even higher THD, quantified as 136.7%.

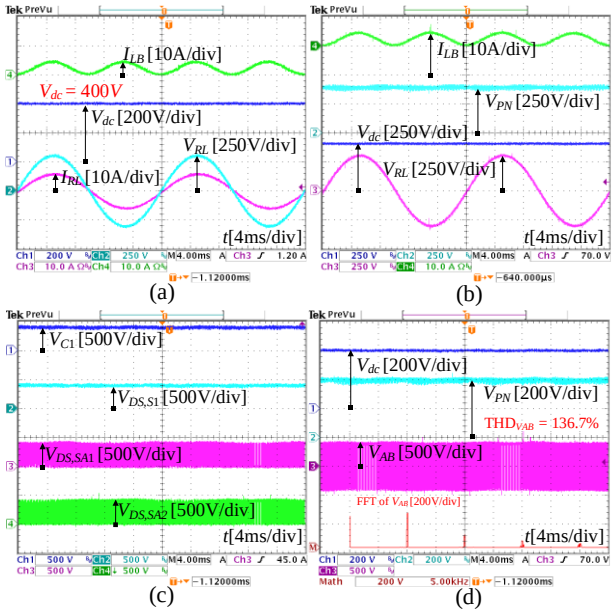

Figure 7: Experimental results with input voltage 400V

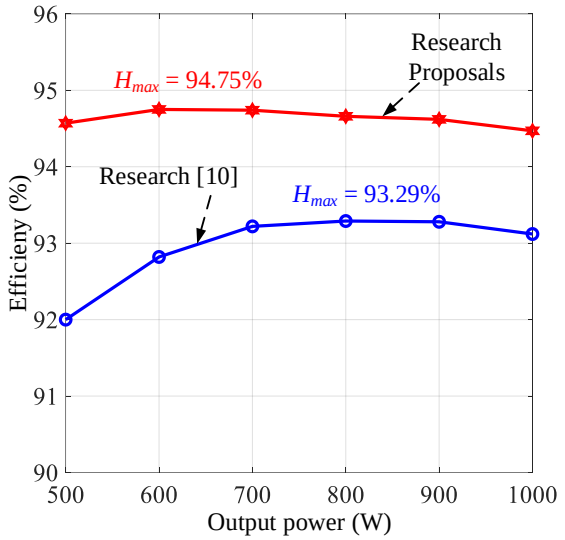

Figure 8: Efficiency comparison between the proposed configuration and the study in [10].

Figure 8 presents the efficiency of the proposed configuration in comparison with the study in [10], measured using a Yokogawa WT3000 power analyzer. Due to the smaller number of passive components, the proposed configuration achieves higher efficiency than [10] at all output power levels. The maximum efficiency obtained within the tested range is 94.75% at 600 W, whereas the configuration in [10] reaches only 93.29% at 800 W.

6. Conclusion

This paper has presented a novel inverter configuration combined with the HPWM modulation technique to optimize power conversion efficiency. The proposed structure demonstrates a significant reduction in power losses by minimizing the number of passive components, thereby enhancing power density and reducing overall system cost. Furthermore, the implementation of the HPWM control algorithm contributes to lowering the switching losses of the power switches and reducing the required DC-link capacitance, which helps to downsize the system and improve its reliability. The effectiveness of the proposed configuration has been verified through experimental results presented in Section 5. With its advantages in efficiency, compactness, and flexible control capability, the proposed inverter topology is considered highly suitable for renewable energy applications, particularly photovoltaic (PV) power systems.

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