A quadratic high-step-up DC–DC converter architecture for renewable energy applications

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Abstract

This paper presents a new quadratic high step-up DC–DC converter featuring a high voltage-gain capability and an optimized component count, suitable for renewable-energy applications. Conventional boost converters achieve high gain only when the duty ratio approaches unity, which results in large conduction losses and reduced efficiency. Existing coupled-inductor solutions often suffer from high input-current ripple and severe voltage spikes, while switched-capacitor or switched-inductor structures require multiple stages, increasing cost and reducing efficiency. The proposed converter addresses these limitations by implementing a quadratic voltage-boost mechanism within a simple topology. It achieves an output voltage 10–13 times higher than the input at a moderate duty ratio of 0.60–0.65, while maintaining continuous input current with low ripple. The operating principles, voltage-gain characteristics, device voltage stresses, and loss mechanisms are analyzed in detail. Simulation results and comparisons with previously published converters confirm that the proposed design offers higher efficiency, reduced device stress, and fewer components, demonstrating its strong potential for practical deployment.

Keywords: *High step–up; Quadratic voltage-boost; Continuous input current; Low component count; Renewable energy*

1. Introduction

The rapid growth of technology has been accompanied by increasing pollution and climate change, primarily driven by excessive dependence on fossil fuels. As a result, alternative energy solutions, especially renewable-energy sources, have gained significant attention as promising substitutes for conventional energy systems [1, 2]. Clean energy sources such as photovoltaic (PV) modules and wind turbines are widely deployed; however, they typically generate low output voltages (20–40 V), whereas many applications, including electric vehicles and DC/AC inverters, require high-voltage levels (380–400 V). High step-up DC–DC converters are therefore essential to bridge this voltage gap, with the conventional boost converter being one of the earliest and most widely studied solutions [3, 4, 5, 6].

Although the theoretical voltage gain of a basic boost converter approaches infinity as the duty ratio approaches unity, practical limitations restrict its performance. As the duty ratio increases, parasitic components in the semiconductor devices and passive elements cause significant efficiency degradation [7]. Consequently, recent research has focused on methods that achieve high voltage gain without relying on extreme duty ratios.

Coupled-inductor (CI) converters are widely used to achieve high step-up voltage gain by increasing the turns ratio of the magnetic structure. Leakage inductance in the coupled inductors is unavoidable, leading to high voltage spikes and increased stress on semiconductor switches during commutation [8]. To mitigate these spikes, voltage-clamp circuits have been proposed, but they increase system complexity and component count [9]. The topology reported in [10] represents a typical CI-based step-up converter that relies on a large turn's ratio and multiple power devices to attain significant voltage gain. However, this design still suffers from high voltage stress on switches, complex magnetic design, and sensitivity to leakage effects, which may limit efficiency and reliability. These limitations highlight the need for alternative step-up converter structures that can achieve high voltage gain while reducing device stress and circuit complexity. To achieve higher voltage gain without using a coupled inductor, switched-capacitor (SC) [11, 12] and switched-inductor (SI) techniques [13] have been developed. Although these methods can provide higher step-up capability, their output voltage and efficiency strongly depend on the number of cascading stages, which increases design cost and reduces overall efficiency. Integrating SC or SI techniques into conventional boost structures can improve the gain [14], but the large number of magnetic cores and components poses challenges for cost optimization. Likewise, combining two CI structures with SI techniques [15] or hybrid SI–SC solutions requiring multiple magnetic cores [16] can achieve higher voltage gain, yet the improvement remains limited. While SC-based converters offer advantages in design cost [17, 18] their achievable gain may still be insufficient for applications demanding significantly higher output voltages. In summary, SC and SI-based step-up techniques provide flexibility in voltage boosting but often require trade-offs among efficiency, component count, and overall system cost.

Recent studies have examined quadratic step-up converter structures as potential solutions for achieving very high voltage gain [19, 20, 21]. Although these topologies offer promising theoretical characteristics, many of them still fall short of meeting practical high-output-voltage requirements.

Motivated by these limitations, this paper proposes a new high step-up converter employing a quadratic voltage-boost mechanism. The proposed structure is optimized for a low component count while maintaining high efficiency. It can achieve an output voltage approximately 10–13 times higher

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than the input with a moderate duty ratio of 0.60–0.65. A notable advantage of the converter is its continuous input-current characteristic, which significantly reduces current ripple and electromagnetic interference, thereby improving the power quality delivered to the load.

The remainder of this paper is organized as follows. Section 2 presents the operating principles and detailed analysis of the proposed topology. Section 3 analyzes the steady-state performance, including voltage gain, voltage stress on power devices, and power loss, and also provides comparative evaluations with previously published converters to highlight its superior characteristics. Section 4 verifies the converter performance and validates the analytical developments through simulation results. Finally, Section 5 summarizes the key findings and discusses the practical implications of the proposed design.

2. Operating principle

The proposed converter topology (PC), shown in Fig. 1, employs two MOSFETs (S_1, S_2) driven simultaneously by the gate signals v_{gs1} and v_{gs2}. The circuit also includes three diodes (D_1, D_2, and the output diode D_o), two single inductors (L_1, L_2), and the capacitors C_1, C_2, which participate in the voltage-boosting process. An output capacitor C_o is used to filter the output voltage.

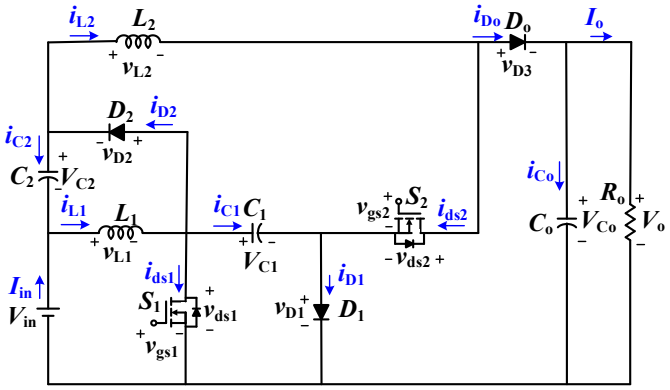
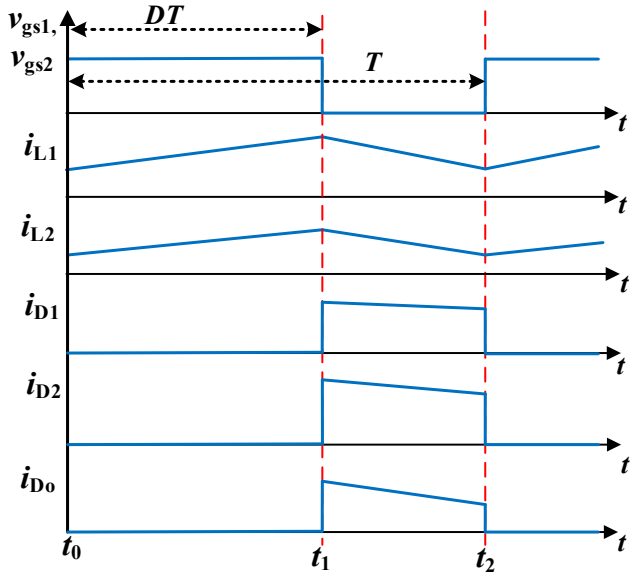
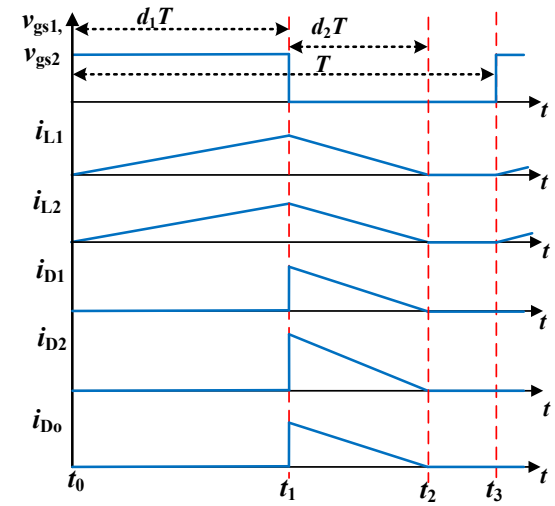


Figure 1: Configuration of the proposed high step-up converter.

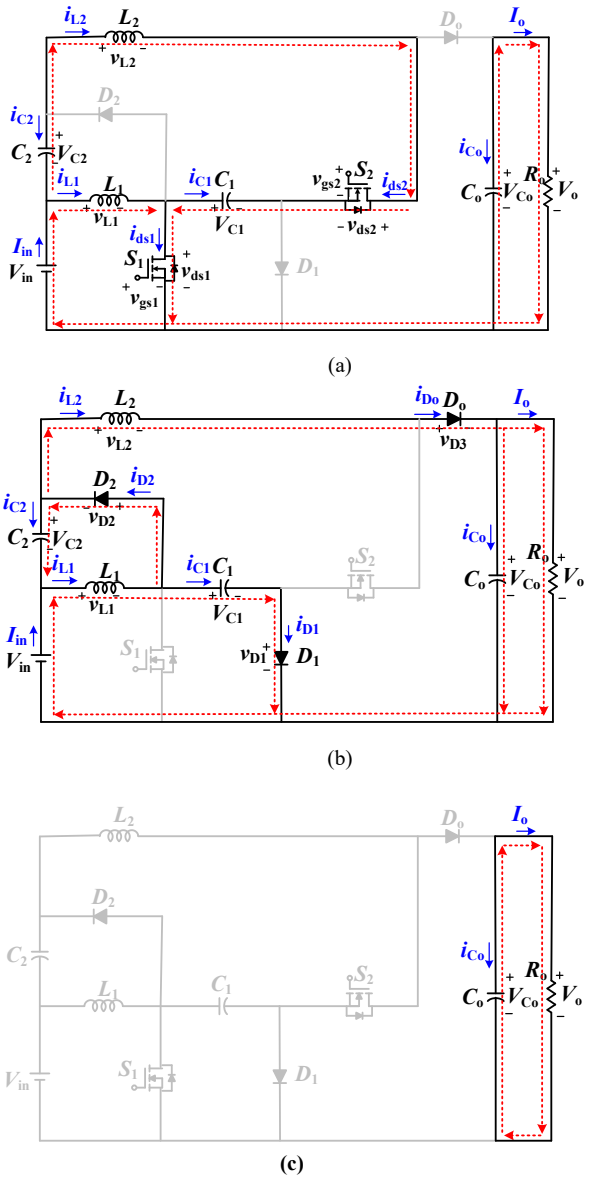


(a)



(b)

Figure 2: Operating waveforms of the PC, (a) in CCM mode, (b) in DCM mode.



(a)

(b)

(c)

Figure 3: Operating diagrams for (a) Mode 1, (b) Mode 2, and (c) DCM mode (Mode 3) of the proposed converter.

2.1. CCM operation

Mode 1 ($t \in [t_0\text{-}t_1]$) in Fig. 3(a): In this mode, both v_{gs1} and v_{gs2} are high, turning on MOSFETs S_1 and S_2 simultaneously. Diodes D_1, D_2, and D_o are reverse-biased and therefore remain OFF. Inductor L_1 is charged from the input source V_{in} through MOSFET S_1, while inductor L_2 is charged from V_{in} together with capacitors C_1 and C_2 through MOSFET S_2. As a result, both inductor currents i_{L1} and i_{L2} increase linearly. Meanwhile, the output capacitor C_o discharges and supplies energy to the load. This mode ends when v_{gs1} and v_{gs2} go low at $t = t_1$.

Mode 2 ($t \in [t_1\text{-}t_2]$) in Fig. 3(b): In this mode, v_{gs1} and v_{gs2} are low, turning OFF both MOSFETs S_1 and S_2. Diodes D_1, D_2 and D_o become forward-biased and conduct. Inductor L_1 releases its stored energy and, together with the input source V_{in}, charges capacitor C_1 through diode D_1. At the same time, L_1 also transfers energy to capacitor C_2 through diode D_2. Inductor L_2 discharges and delivers energy to the output capacitor C_o and the load. This mode ends when v_{gs1} and v_{gs2} return to the high level at $t = t_2$.

2.2. DCM operation

In DCM operation, the converter includes Mode 1 and Mode 2 of CCM, along with an additional operating mode, Mode 3, as illustrated in Fig. 3(c). In this mode, the energy stored in both inductors decreases to zero; consequently, the voltage conversion ratio becomes independent of the duty cycle D. The operating waveforms in DCM are shown in Fig. 2(b).

Operating modes I and II are identical to those in CCM. The distinction arises in Mode 3 ($t \in [t_2\text{-}t_3]$), during which all diodes are reverse-biased, and both inductors carry zero current. In this mode, the output capacitor C_O solely supplies energy to the load.

3. Analysis of the proposed converter

3.1. Voltage gain

a) Voltage Gain Analysis in CCM:

Applying Kirchhoff's II law to the circuit when MOSFETs S_1 and S_2 are ON, as shown in Fig. 3(a), the following voltage equations are obtained:

$$v_{L1} = V_{in} \quad (1)$$

$$v_{L2} = V_{C1} + V_{C2} + V_{in} \quad (2)$$

$$V_O = V_{Co} \quad (3)$$

When both MOSFETs S_1 and S_2 are OFF, as shown in Fig. 3(b), applying Kirchhoff's II law yields the following voltage equations:

$$v_{L1} = V_{in} - V_{C1} \quad (4)$$

$$v_{L1} = -V_{C2} \quad (5)$$

$$v_{L2} = V_{C1} - V_O \quad (6)$$

From (1) and (4), by applying the volt–second balance principle to inductor L_1, the following equation is obtained:

$$\frac{1}{T}\int_0^T v_{L1}dt = \frac{1}{T}\int_0^{DT} V_{in}dt + \frac{1}{T}\int_{DT}^T (V_{in} - V_{C1})dt$$

$$= DV_{in} + (1-D)(V_{in} - V_{C1}) = 0 \quad (7)$$

From (7), the expression for V_{C1} can be obtained as follows:

$$V_{C1} = \frac{V_{in}}{1-D} \quad (8)$$

The voltage expression of capacitor C_2, derived from (4), (5), and (8), is given as follows:

$$V_{C2} = V_{C1} - V_{in} = \frac{V_{in}}{1-D} - V_{in} = \frac{DV_{in}}{1-D} \quad (9)$$

From (2) and (6), by applying the volt–second balance principle to inductor L_2, the following equation is obtained:

$$\frac{1}{T}\int_0^T v_{L2}dt = \frac{1}{T}\int_0^{DT}(V_{C1} + V_{C2} + V_{in})dt + \frac{1}{T}\int_{DT}^T (V_{C1} - V_o)dt$$

$$= D(V_{C1} + V_{C2} + V_{in}) + (1-D)(V_{C1} - V_O) = 0 \quad (10)$$

Substituting (8) and (9) into (10), the output-voltage expression V_O is obtained as follows:

$$V_O = \frac{V_{C1} + DV_{C2} + DV_{in}}{1-D} = \frac{V_{in} + D^2V_{in} + D(1-D)V_{in}}{(1-D)^2} \quad (11)$$

Based on (11), the voltage gain of the proposed converter can be written as follows:

$$\frac{V_O}{V_{in}} = \frac{1+D}{(1-D)^2} \quad (12)$$

b) Voltage Gain Analysis in DCM:

In DCM operation, the converter includes an additional operating interval in which the inductor currents fall to zero, resulting in a different voltage gain characteristic compared with CCM. For DCM analysis, d_1T corresponds to the time interval during which switches S_1 and S_2 are turned ON, whereas d_2T indicates the conduction interval of diode D_1 prior to the onset of Mode 3.

By applying the voltage balance theorem to inductor L_1, the following equation is derived:

$$\frac{1}{T}\int_0^{d_1T} V_{in}dt + \frac{1}{T}\int_{d_1T}^{(d_1+d_2)T}(V_{in} - V_{C1})dt = d_1V_{in} + d_2(V_{in} - V_{C1}) = 0 \quad (13)$$

The voltage equation across C_1 can be derived from (13) as follows:

$$V_{C1} = \frac{d_1+d_2}{d_2}V_{in} \quad (14)$$

The voltage equation across C_2 is determined as follows:

$$V_{C2} = V_{C1} - V_{in} = \frac{d_1+d_2}{d_2}V_{in} - V_{in} = \frac{d_1}{d_2}V_{in} \quad (15)$$

By applying the voltage balance theorem to L_2, the following voltage equation is obtained:

$$\frac{1}{T}\int_0^{d_1T}(V_{C1} + V_{C2} + V_{in})dt + \frac{1}{T}\int_{d_1T}^{(d_1+d_2)T}(V_{C1} - V_O)dt = d_1(V_{C1} + V_{C2} + V_{in}) + d_2(V_{C1} - V_O) = 0 \quad (16)$$

Substituting equations (14) and (15) into equation (16), the output voltage equation V_o is obtained as follows:

$$V_O = \frac{(2d_1+d_2)(d_1+d_2)}{d_2^2}V_{in} \quad (17)$$

Based on (17), the voltage gain under DCM is obtained as follows:

$$M_{DCM} = \frac{V_O}{V_{in}} = \frac{(2d_1+d_2)(d_1+d_2)}{d_2^2} \quad (18)$$

3.2. Voltage stress on components

When S_1 and S_2 are in the OFF, as shown in Fig. 3(b), switch S_1 becomes clamped in parallel with capacitor C_1 through diode D_1, and switch S_2 is clamped in parallel with the output capacitor C_o through diodes D_1 and D_o. Therefore, the voltage stresses on the two switches are given as follows:

$$V_{S1} = V_{C1} = \frac{V_{in}}{1-D} = \frac{1-D}{1+D}V_O \quad (19)$$

$$V_{S2} = V_O = \frac{1+D}{(1-D)^2}V_{in} = V_O \quad (20)$$

Accordingly, the voltage stresses on the diodes can be determined as follows:

$$V_{D1} = V_{C1} = \frac{V_{in}}{1-D} = \frac{1-D}{1+D}V_O \quad (21)$$

$$V_{D2} = V_{C2} + V_{in} = \frac{V_{in}}{1-D} = \frac{1-D}{1+D}V_O \quad (22)$$

$$V_{Do} = V_{C1} + V_O = \frac{2}{(1-D)^2}V_{in} = \frac{2}{1+D}V_O \quad (23)$$

3.3. Inductor design

By applying Kirchhoff's I law to Fig. 1, the following current equation is obtained:

$$i_{L1} = i_{C2} + I_{in} \quad (24)$$

$$i_{Do} = i_{Co} + I_o \quad (25)$$

$$i_{L2} = i_{ds2} + i_{Do} \quad (26)$$

Based on (24), the following equation is obtained:

$$\frac{1}{T}\int_0^T i_{L1}dt = \frac{1}{T}\int_0^T (i_{C2} + I_{in})dt = I_{in} \quad (27)$$

The average current flowing through L_1 can be determined from (27) as follows:

$$I_{L1\_ave} = I_{in} \quad (28)$$

The average current through diode D_o can be determined from (25) as follows:

$$I_{Do\_ave} = \frac{1}{T}\int_0^T i_{Do}dt = \frac{1}{T}\int_{DT}^T i_{Do}dt = \frac{1}{T}\int_0^T (i_{Co} + I_o)dt = I_o \quad (29)$$

When $t \in [DT\text{-}T]$ in Fig. 3(b), and using (26) and (29), the following expression is obtained:

$$\frac{1}{T}\int_{DT}^T i_{L2}dt = \frac{1}{T}\int_{DT}^T (i_{ds2} + i_{Do})dt = \frac{1}{T}\int_{DT}^T (i_{Do})dt = I_o \quad (30)$$

The average current through inductor L_2 can be determined from (30) as follows:

$$I_{L2\_ave} = \frac{I_o}{1-D} \quad (31)$$

Together with the inductor-voltage expression of L_1 for $t \in$ [0-DT] given in (1), the ripple equation of inductor L_1 can be expressed as follows:

$$\Delta I_{L1} = \frac{1}{T}\int_0^{DT} di_{L1} = \frac{1}{T}\int_0^{DT} \frac{v_{L1}}{L_1}dt = \frac{DTV_{in}}{L_1} \quad (32)$$

During the interval $t \in$ [0-DT], the current ripple of L_2 can be expressed as follows:

$$\Delta I_{L2} = \frac{1}{T}\int_0^{DT} di_{L2} = \frac{1}{T}\int_0^{DT} \frac{v_{L2}}{L_2}dt = \frac{DT(V_{C1} + V_{C2} + V_{in})}{L_2} = \frac{2DTV_{in}}{(1-D)L_2} \quad (33)$$

The minimum currents through L_1 and L_2 are given by:

$$I_{L1\_min} = I_{L1\_ave} - \frac{\Delta I_{L1}}{2} \quad (34)$$

$$I_{L2\_min} = I_{L2\_ave} - \frac{\Delta I_{L2}}{2} \quad (35)$$

At the boundary condition mode, the minimum current in both inductors reaches zero ($I_{L1\_min} = 0$ and $I_{L2\_min} = 0$). Therefore, using (28), (31), (32), and (33), the following condition is derived to maintain CCM operation:

$$I_{L1} \geq \frac{\Delta I_{L1}}{2} \rightarrow L_1 \geq \frac{DTV_{in}}{2I_{in}} \quad (36)$$

$$I_{L2} \geq \frac{\Delta I_{L2}}{2} \rightarrow L_2 \geq \frac{DTV_{in}}{I_o} \quad (37)$$

From equations (36) and (37), the minimum inductance curves for L_1 and L_2 are presented in Fig. 4. It can be observed that under identical operating conditions input voltage, switching frequency, and power level inductor L_2 requires a higher inductance value to achieve CCM than L_1. Consequently, the design must use different inductance values, specifically with L_2 larger than L_1, to maintain both inductors in continuous conduction mode.

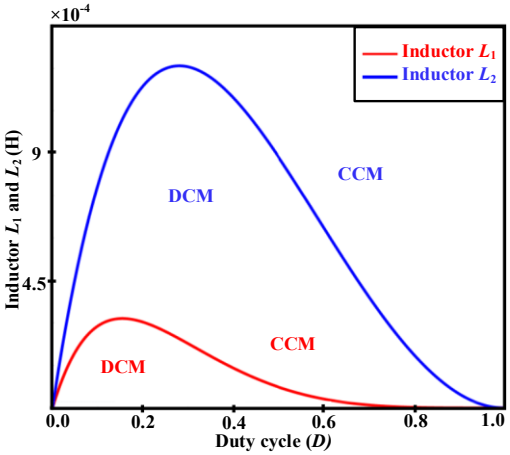


Figure 4: The inductance curves for L_1 and L_2.

3.4. Power loss analysis

The loss analysis is calculated based on the average current and root mean square (RMS) current of the components. Furthermore, each component possesses an equivalent series resistance, which contributes to the power loss of the proposed structure. Based on the ON and OFF states of the switch, the component current analysis is presented in Table 1 as follows:

Table 1: Average current and RMS current of components.

Diode			Capacitor		
	Average current	RMS curent		Average current	RMS curent
D_1 (C6D10065G) $r_{D1} = 50$ mΩ $V_{F\_D1} = 1.27$ V	$\frac{DI_o}{1-D}$	$\frac{I_oD}{\sqrt{(1-D)^3}}$	C_1 $r_{C1} = 170$ mΩ	0	$\frac{I_o\sqrt{D(1-D)}}{(1-D)^2}$
D_2 (C6D10065G) $r_{D2} = 50$ mΩ $V_{F\_D2} = 1.27$ V	$\frac{I_o}{1-D}$	$\frac{I_o}{\sqrt{(1-D)^3}}$	C_2 $r_{C2} = 170$ mΩ	0	$\frac{I_o\sqrt{D}}{\sqrt{(1-D)^3}}$
D_o(C6D10065G) $r_{Do} = 50$ mΩ $V_{F\_Do} = 1.27$ V	I_o	$\frac{I_o}{\sqrt{1-D}}$	C_o $r_{Co} = 65$ mΩ	0	$\frac{I_o\sqrt{D}}{1-D}$
MOSFET			Inductor		
S_1(IXFH120N20P) $r_{ds1\_ON} = 22$ mΩ $t_{r1} = 35$ ns $t_{f1} = 31$ ns	$\frac{2D}{(1-D)^2}I_o$	$\frac{2I_o\sqrt{D}}{(1-D)^2}$	L_1 $r_{L1} = 25$ mΩ	$\frac{1+D}{(1-D)^2}I_o$	$\frac{1+D}{(1-D)^2}I_o$
S_2(GAN041-650WSB) $r_{ds2\_ON} = 35$ mΩ $t_{r2} = 14$ ns $t_{f2} = 17$ ns	$\frac{D}{1-D}I_o$	$\frac{I_o\sqrt{D}}{1-D}$	L_2 $r_{L1} = 185$ mΩ	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$

Based on Table 1, the component loss distribution at an output power level of P_o = 300W is presented in Table 2 as follows:

Table 2: Component loss distribution.

Components		Loss Formula	Power loss (W)
Diodes (42.73%)	D_1	$r_{D1}.I^2_{D1\_RMS} + V_{F\_D1}.I_{D1\_ave}$	1.75
	D_2	$r_{D2}.I^2_{D2\_RMS} + V_{F\_D2}.I_{D2\_ave}$	3.02
	D_o	$r_{Do}.I^2_{Do\_RMS} + V_{F\_Do}.I_{Do\_ave}$	1.02
MOSFETs (21.70%)	S_1	$r_{ds1\_ON}.I^2_{ds1\_RMS} + \frac{1}{2}v_{ds1}.I_{S1\_ave}(t_{r1} + t_{f1})f$	2.47
	S_2	$r_{ds2\_ON}.I^2_{ds2\_RMS} + \frac{1}{2}v_{ds2}.I_{S2\_ave}(t_{r2} + t_{f2})f$	0.47
Capacitors (17.20%)	C_1	$r_{C1}.I^2_{C1\_RMS}$	1.08
	C_2	$r_{C2}.I^2_{C2\_RMS}$	1.08
	C_o	$r_{Co}.I^2_{Co\_RMS}$	0.17
Inductors (18.37%)	L_1	$r_{L1}.I^2_{L1\_RMS}$	1.77
	L_2	$r_{L2}.I^2_{L2\_RMS}$	0.72
Total loss			13.55

Based on the loss analysis, the efficiency curve is presented in Fig. 5. A peak efficiency of 96.55% is achieved at 160 W, while the full-load efficiency at 300 W is 95.68%. The efficiency curve does not remain flat, as it is affected by losses such as switching loss, conduction loss, and parasitic losses.

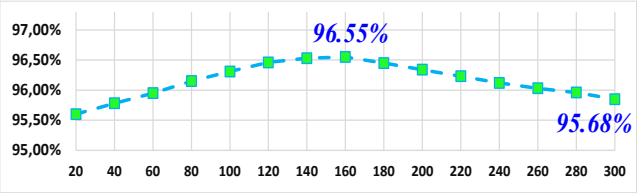


Figure 5: The efficiency curve of the proposed converter.

4. Performance comparison with state-of-the-art high step-up converters

To highlight the advantages of the proposed topology, a comprehensive comparison with previously reported high step-up DC–DC converters is conducted based on key performance metrics, including the number of power switches (MOSFETs), diodes, inductors, and the total component count. In addition, the voltage-gain characteristics and the normalized voltage stress on the main MOSFET are summarized in Table 3. Comparative plots of voltage gain and MOSFET reverse voltage as functions of the duty ratio are presented in Figs. 6 and 7, respectively, to clearly illustrate the performance differences between the proposed converter and existing designs.

As shown in Table 3, Figs. 6, and 7, the proposed topology achieves a higher voltage gain than most previously reported converters at moderate duty ratios (D = 0.6–0.65). Although the proposed converter does not strictly minimize the number of components among all topologies, it employs the same total component count as the converters reported in [17, 18, 19, 20, 21], while requiring fewer components than the converters in [14, 15].

Table 3: Comparison of the PC with advanced topologies.

Ref.	No. of components					VG V_o/V_{in}	Voltage stress on the main switch v_{ds}/V_o
	Switch (S)	Diode (D)	Capacitor (C)	Inductor (L)	Total		
[14]	1	3	6	4	14	$\frac{3D}{1-D}$	$\frac{1}{3D}$
[15]	2	7	1	4	14	$\frac{1+2D}{1-D}$	$\frac{2+D}{2+4D}$
[16]	2	2	3	3	10	$\frac{1+3D}{1-D}$	$\frac{1}{1+3D}$
[17]	2	3	3	2	10	$\frac{3+D}{1-D}$	$\frac{1}{3+D}$
[18]	2	3	3	2	10	$\frac{3+D}{1-D}$	$\frac{1}{3+D}$
[19]	2	3	3	2	10	$\frac{2D}{(1-D)^2}$	$\frac{1-D}{2D}$
[20]	2	3	3	2	10	$\frac{1+D}{D(1-D)}$	$\frac{D}{1+D}$
[21]	2	3	3	2	10	$\frac{2-D}{(1-D)^2}$	$\frac{1}{2-D}$
The PC	**2**	**3**	**3**	**2**	**10**	$\mathbf{\frac{1+D}{(1-D)^2}}$	$\mathbf{\frac{1-D}{1+D}}$

Compared with the topologies in [14] and [15], the proposed converter significantly reduces the overall component count while simultaneously achieving lower voltage stress on the main MOSFET. This reduced device stress improves system reliability and enables the use of lower-voltage-rated MOSFETs with smaller on-state resistance, thereby contributing to improved conversion efficiency.

In comparison with the converters reported in [16, 17, 18], although a similar number of magnetic components and energy-transfer stages is required, the proposed topology provides a higher voltage-gain ratio. This enhancement is primarily attributed to the effective exploitation of a quadratic voltage-boosting mechanism combined with continuous input-current operation, which enables efficient voltage amplification under practical duty ratios.

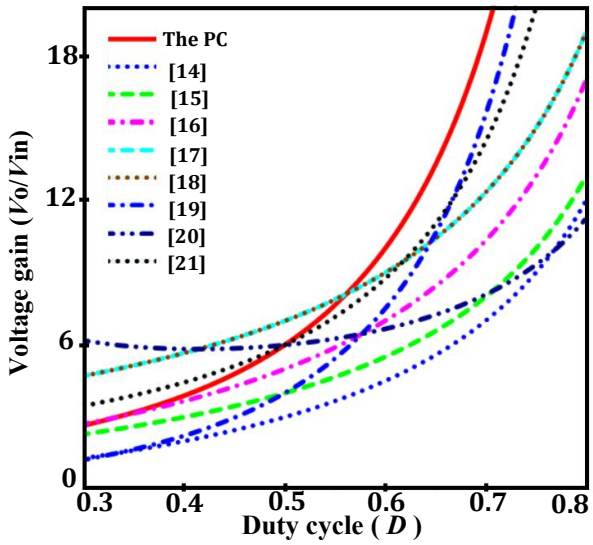


Figure 6: Voltage-gain comparison with previously published converters.

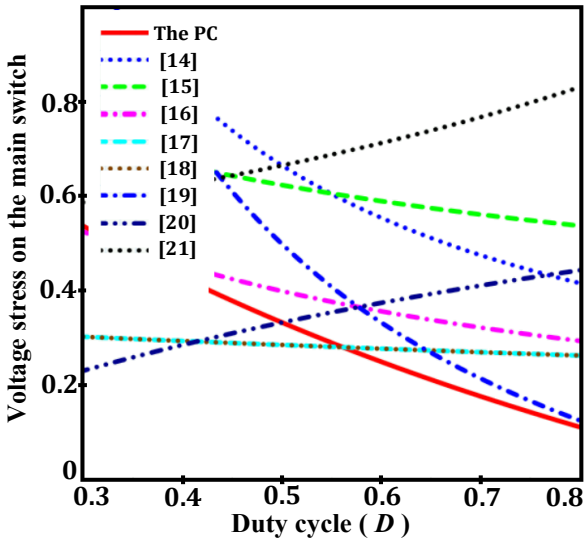


Figure 7: Comparison of main-switch voltage stress with previously published converters.

It is worth noting that the proposed converter employs the same fundamental quadratic charge–discharge mechanism as previously reported quadratic and hybrid switched-capacitor/inductor converters [19, 20, 21]. Therefore, the novelty lies not in a new operating principle, but in the structural organization of the existing quadratic mechanism. Unlike those converters, whose voltage-gain expressions include multiple voltage-subtraction terms that limit gain growth when $D >$ 0.5, the proposed topology ensures that all intermediate capacitors actively participate in the boosting process during each switching cycle. As a result, a steeper voltage-gain characteristic is achieved in the high-duty-ratio region.

Moreover, the intrinsic voltage-partitioning characteristic ensures even voltage sharing among power devices. Consequently, the proposed converter exhibits lower normalized voltage stress on the main MOSFET compared with the converters in [19, 20, 21] under the same duty ratio and voltage gain. Since the main switch operates on the low-side input path with high current, minimizing its voltage stress allows the use of a low-$R_{DS(on)}$ switch, thereby reducing conduction loss and enhancing efficiency.

Overall, the proposed converter offers an improved performance trade-off by achieving higher voltage gain and reduced voltage stress on the main switch without increasing circuit complexity. These advantages make it a promising candidate for high step-up DC–DC conversion applications requiring high efficiency, moderate duty ratios, and reliable operation.

5. Simulation-based performance evaluation using SIMetrix–SIMPLIS

The PC was simulated and evaluated in the SIMetrix–SIMPLIS environment to validate the theoretical analyses. The simulation conditions are summarized in Table 4. The schematic of the simulated topology is shown in Fig. 8 and the corresponding simulation waveforms are presented in Fig. 9.

Table 4: Key parameters used in the simulation.

Device name	Value
Output power (P_o)	300 W
Output voltage (V_o)	400 V
Input voltage (V_{in})	36 V
Switching frequency (f)	50 kHz
Inductor L_1	400 µH
Inductor L_2	900 µH
Capacitors C_1 and C_2	68 µF
Capacitor C_o	330 µF

Based on the results shown in Fig. 9, it can be observed that in Fig. 9(a), with a duty ratio of D = 62%, the reverse voltages across S_1 and S_2 reach 94 V and 400 V, respectively, which is fully consistent with the theoretical analyses previously derived in (13) and (14). The inductor-current waveforms confirming continuous conduction mode are presented in Fig. 9(b). The voltage stresses on the diodes are also validated through Figs. 9(c) and 9(d). In addition, the output-voltage ripple is very small, with $\Delta V_O = 0.015\,V$, demonstrating a stable output voltage suitable for renewable-energy applications.

To verify the continuous input current characteristic, the input current i_{in} is directly measured at the input source terminal, and the corresponding waveform is shown in Fig. 9(e). As can be observed i_{in} remains strictly positive over the entire switching period, with a minimum value of approximately 4.08 A, thereby confirming continuous input current operation.

The dynamic performance of the proposed converter was evaluated via MATLAB/Simulink simulations under varying input voltage and load conditions, which can be described as follows:

- Input voltage variation: The input voltage V_{in} was varied from 36 V to 48 V while maintaining a 300 W output and V_O = 400 V. Using the feedback control scheme, the transient responses in Fig. 10(a) indicate that the output voltage quickly recovers and remains stable, confirming the robustness of the control system.
- Load variation: Step changes in load were applied at 50% load (I_O = 0.375 A) and full load (I_O = 0.75 A) with a fixed input of V_{in} = 36 V. The responses in Fig. 10(b) show that the output voltage rapidly settles to the reference value after each load change, demonstrating effective feedback control and stable operation.

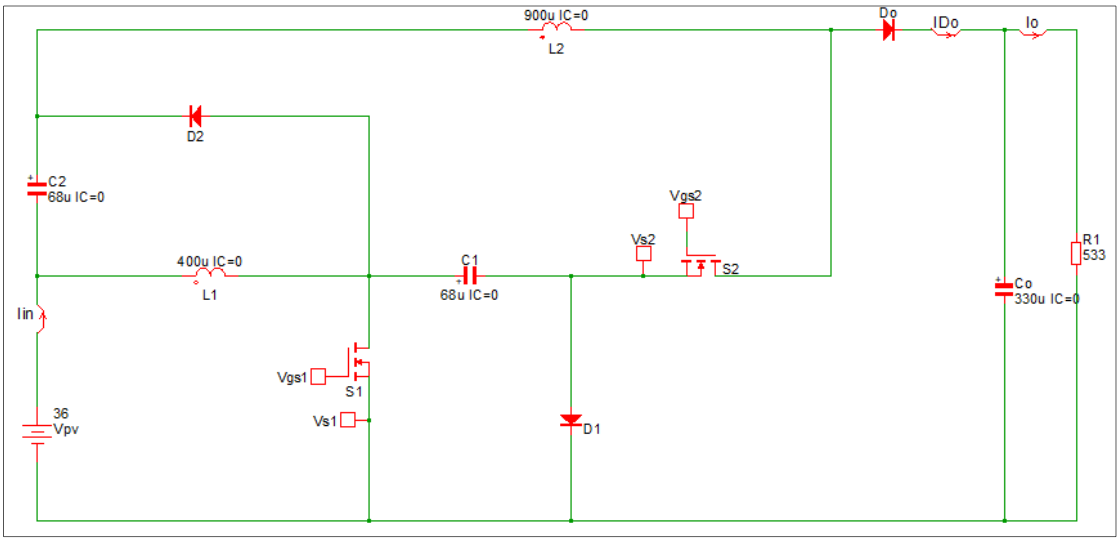
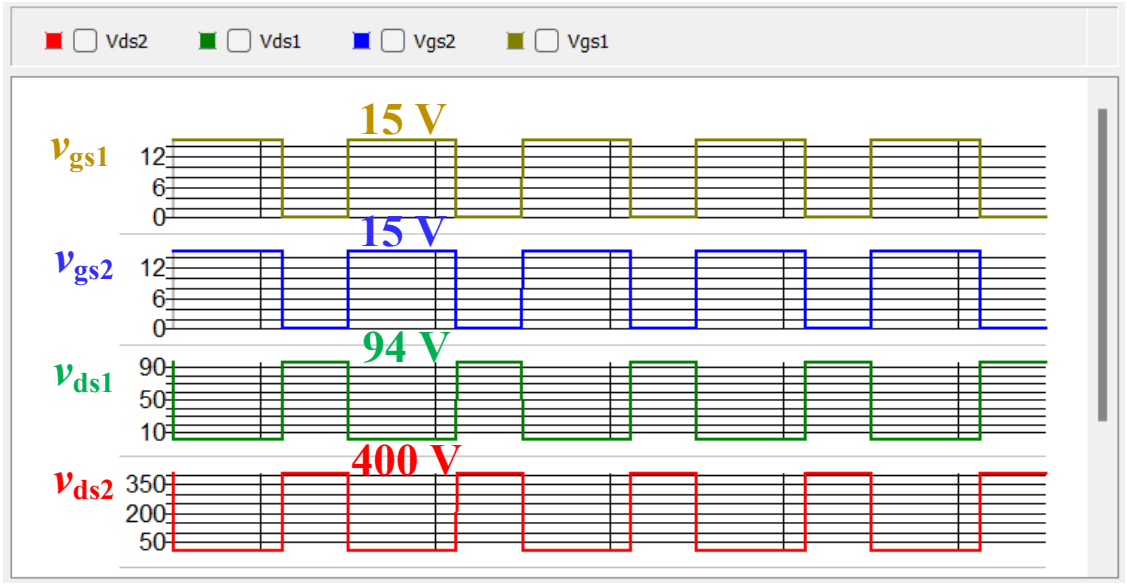
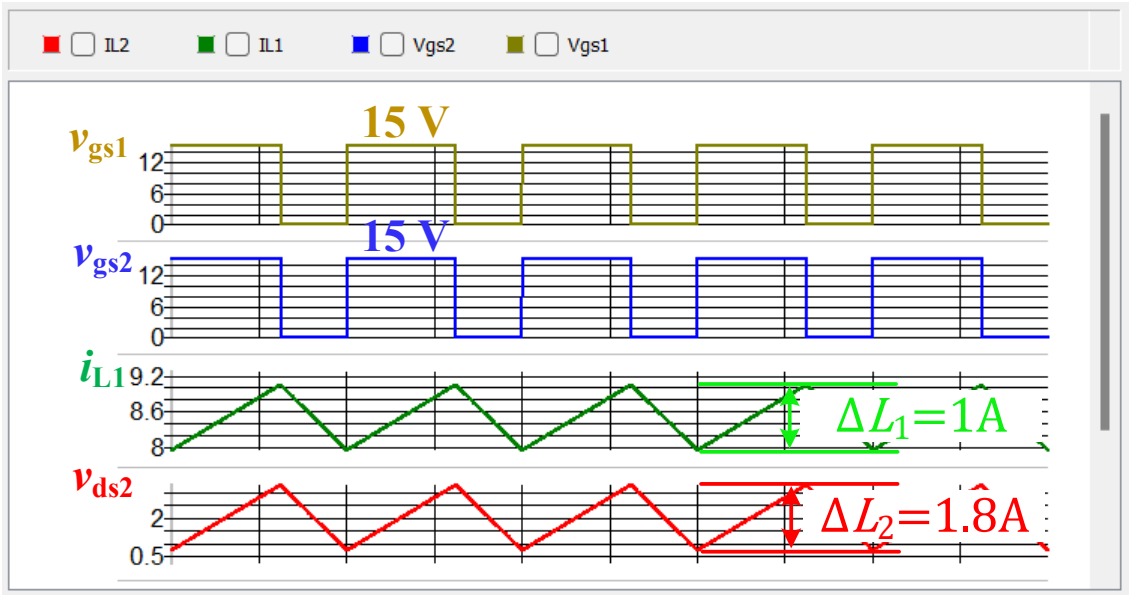


Figure 8: Simulation schematic of the PC in SIMetrix–SIMPLIS.



(a) v_{gs1}, v_{gs2}, v_{ds1} and v_{ds2}.



(b) v_{gs1}, v_{gs2}, i_{L1} and i_{L2}.

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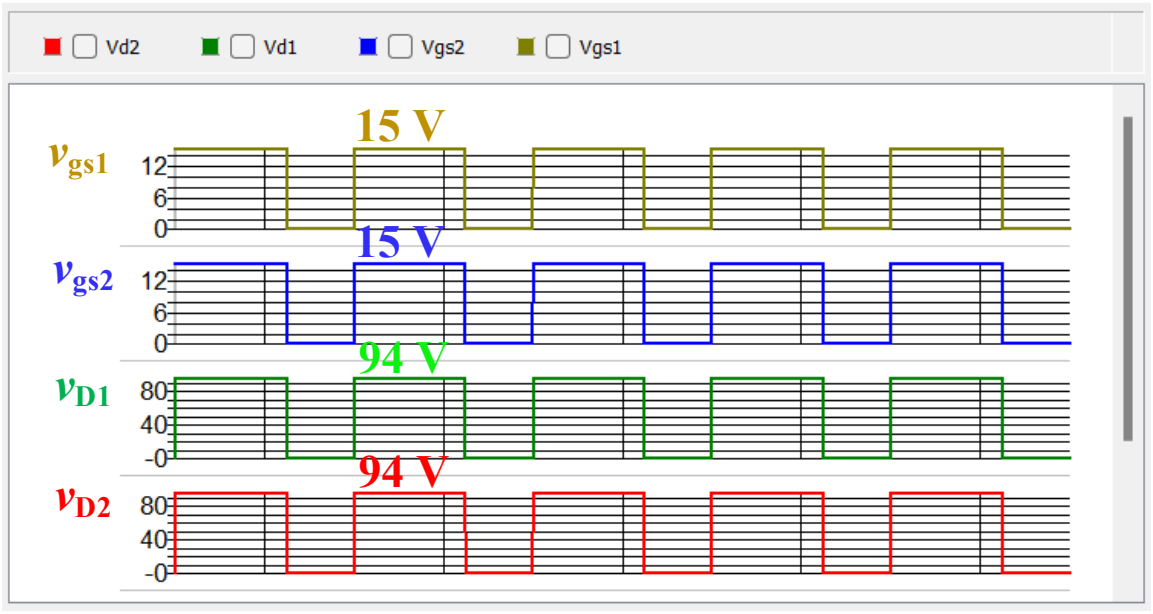
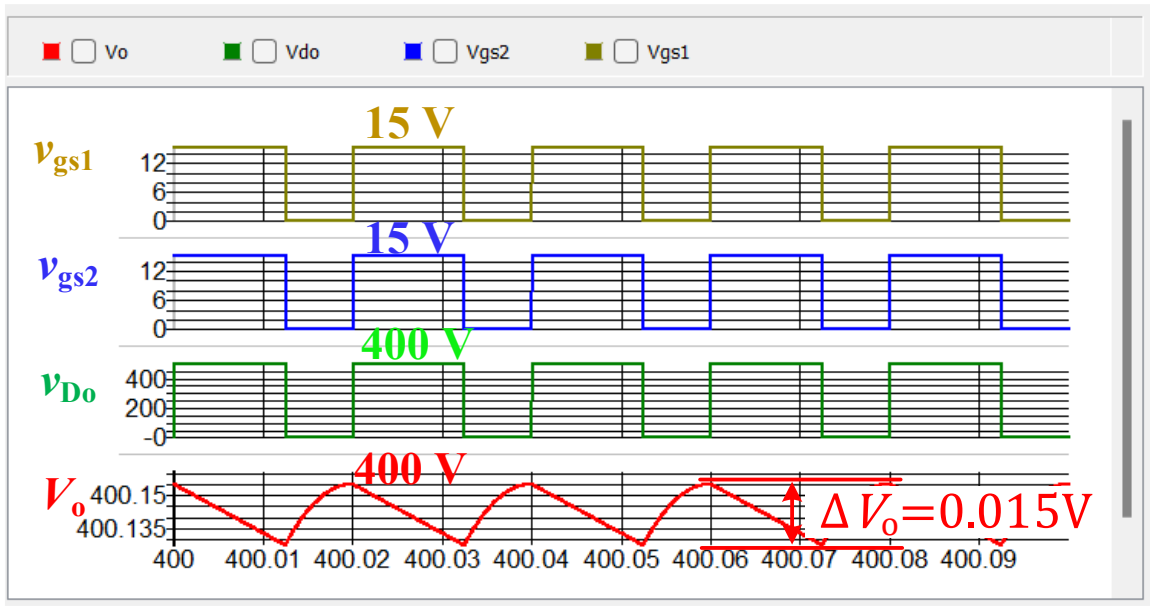
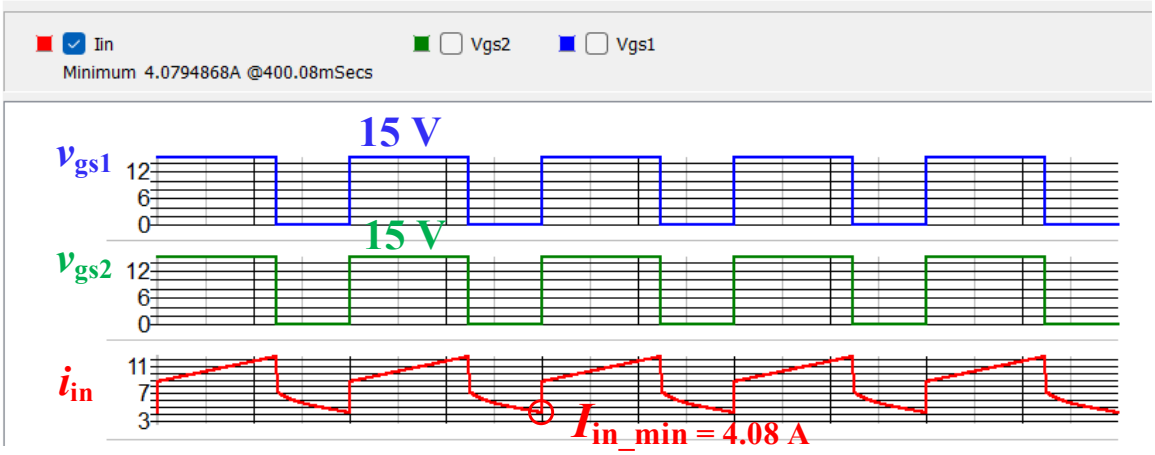


(c) v_{gs1}, v_{gs2}, v_{D1} and v_{D2}.

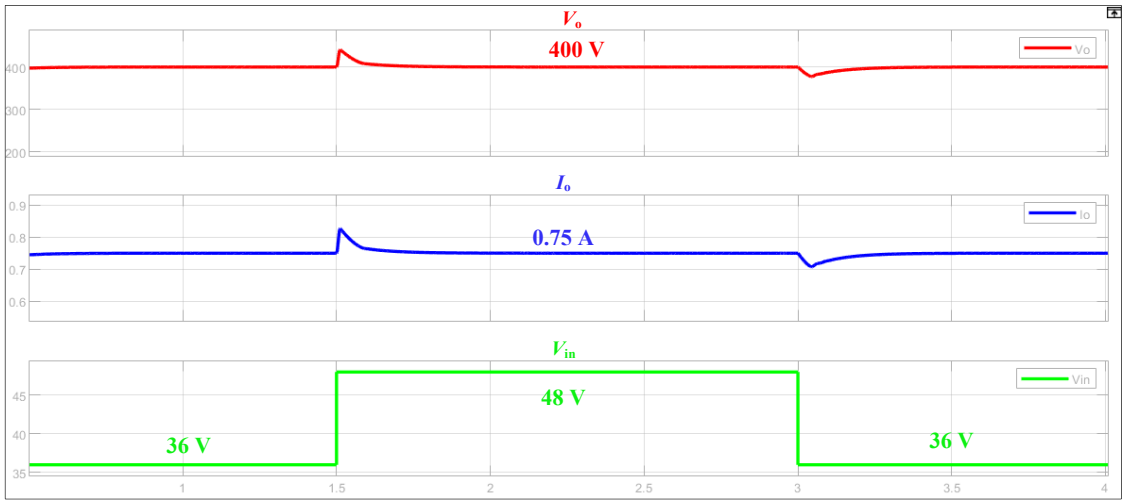


(d) v_{gs1}, v_{gs2}, v_{Do} and V_o.

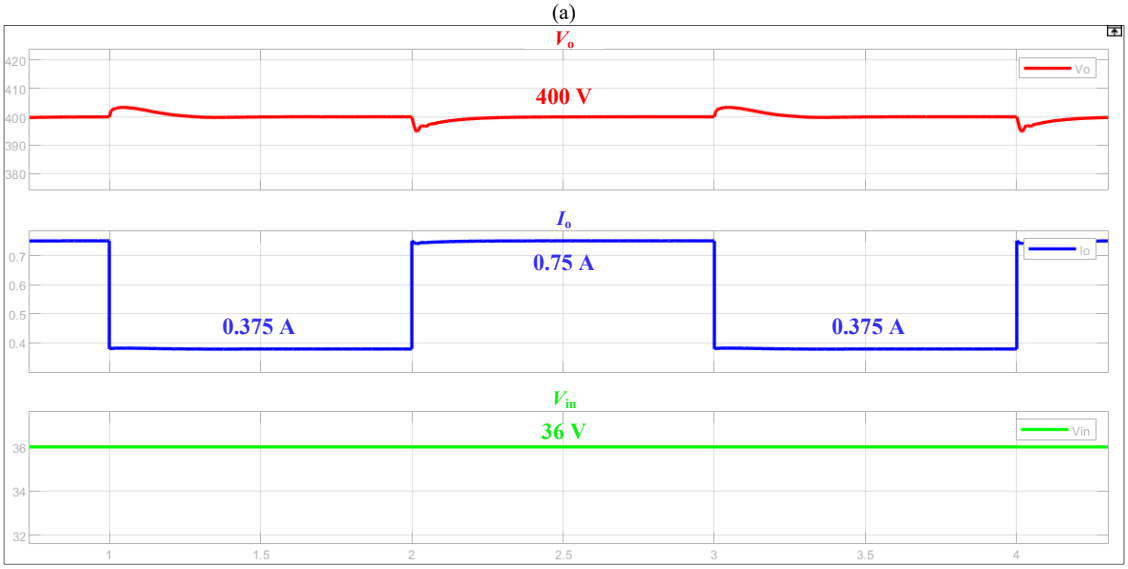


(e) v_{gs1}, v_{gs2}, v_{Do} and i_{in}.

Figure 9: SIMetrix–SIMPLIS simulation waveforms of the PC.



(a)



(b)

Figure 10: Dynamic response under (a) input voltage variation and (b) load variation.

6. Conclusion

This paper has presented a quadratic high step-up DC–DC converter with an optimized design that combines a low component count with a high voltage-gain capability. Analytical derivations and simulation results confirm that the proposed topology achieves an output voltage 10–13 times higher than the input at a moderate duty ratio (D = 0.6–0.65), while maintaining continuous input current with reduced ripple and electromagnetic interference. The converter attains a high efficiency above 95%, and the voltage stress on the main MOSFETs is significantly reduced, thereby improving device reliability and overall system robustness. Comparative evaluation with previously published converters demonstrates that the proposed design offers higher efficiency, stable output voltage, and fewer components. These results verify that the PC is an effective and reliable solution for applications requiring a stable high-voltage supply, particularly in renewable-energy systems.

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