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A Single-Stage Neutral Point Clamp Inverter with Reduced Voltage Stresses on Power Elements

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Abstract

In this paper, a topology incorporating the DC-link type quasi-switched boost network with the traditional three-level neutral point clamped inverter is presented. The third harmonic injection method is proposed to provide some benefits such as: enhancing the modulation index or improving the voltage gain. Moreover, the stress voltage on power devices like capacitors, diodes, and switches is decreased, significantly. The mathematic analysis is detailed to produce the output voltage equations for the proposed converter. The comparison between the proposed topology to conventional quasi-switched boost neutral point clamped inverter topology is carried out. Simulation and experimental results are conducted to verify the accuracy of the inverter.

Keywords: *PWM strategy; Quasi-switched boost inverter, Shoot-through, Three-level inverter, T-type inverter.*

Symbol

Symbol	Unit	Meaning
V_{in}	V	Input voltage
i_o	A	Output current
m		Modulation index
V_{ag}	V	Output phase voltage
V_{a0}	V	Pole voltage
V_{ab}	V	The line-to-line voltages
D_0		Duty cycle
d		The duty cycle of the two switches impedance network

Nomenclature

PWM	Pulse width modulation
DSP	Digital signal processing
IGBT	Insulated-gate bipolar transistor
DC	Direct Current
AC	Alternating Current
THD	Total Harmonic Distortion
ST	Shoot-through

Tóm tắt

Trong bài báo này, một cấu hình kết hợp mạng tăng áp tựa khóa chuyển mạch dạng DC-link với nghịch lưu diode kẹp ba bậc truyền thống được trình bày. Phương pháp tiêm hài bậc ba được đề nghị để tạo ra một số lợi ích như: tăng cường chỉ số điều chế hoặc cải tiến độ lợi điện áp. Kết quả, điện áp đặt trên các phần tử công suất như: các tụ điện, các diode và các khóa chuyển mạch được giảm mạch cách đáng kể. Phân tích toán học được chi tiết hóa để tạo ra các phương trình điện áp ngõ ra cho nghịch lưu đề nghị. Sự so sánh giữa cấu hình đề nghị với cấu hình nghịch lưu tăng áp ba bậc truyền thống được thực hiện. Kết quả mô phỏng và thực nghiệm được thực hiện để xác minh tính chính xác của lý thuyết hoạt động bộ nghịch lưu.

1. Introduction

Recently, the multilevel voltage source inverter (VSI) is used in a wide range of applications like photovoltaic (PV) systems, wind power, hybrid electric vehicle (HEV), fuel cell, uninterrupted power supply, etc [1]-[3]. However, traditional VSI topologies behave as a buck converter which produces a smaller peak-to-peak output voltage than the DC-link voltage [4]. To overcome these limitations, the Z-source (ZS) topology was explored in [5]. By using one more diode, two additional inductors, and two additional capacitors, this configuration is known as a single-state inverter which provides a buck-boost voltage capability and ST immunity. The words of literature [6], [7] explored the combination between the ZS network and the conventional three-level NPC inverter (TL-NPCI). The literature [8], [9] proposed a novel type of impedance network called quasi-Z-source (qZS) to improve the limitations of ZS network. These studies connected two identical qZS networks in cascade form to produce a three-level voltage at the output terminal. Therefore, it improves the quality of output voltage. However, it also increases the number of passive components such as capacitors and inductors. As a result, the weight, size, and cost of the system are increased significantly. With using one more active switch, the quasi-switched boost (qSB) network saves one inductor and one capacitor compared to qZS topology whereas the boost factor is maintained [10]. The literature [11] presented a pulse with modulation (PWM) scheme based on the phase shift carrier method to reduce the inductor current ripple and enhance the boost factor of the converter. The three-level quasi-switched boost NPC inverter in [12] uses two more extra switches but reduces a large number of passive

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components. Although the three-level boost NPC inverter in [12] has good performance in terms of reducing passive components and providing continuous input current, it uses two inductors and two DC voltage sources or a single split DC voltage source, which increases the volume and price. In the literature [13], a combination of the three level T-Type inverter (3L-T^{2}I) with the qSB network was discussed. In this study, two identical qSB networks were connected in cascade form with one inductor less to create a three-level voltage at output voltage. Moreover, a PWM strategy to reduce the inductor current ripple as well as enhancing the boost factor of the converter was also presented.

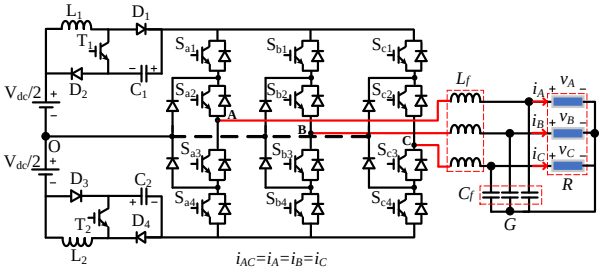

Fig.1 *Modified qSB-NPC inverter.*

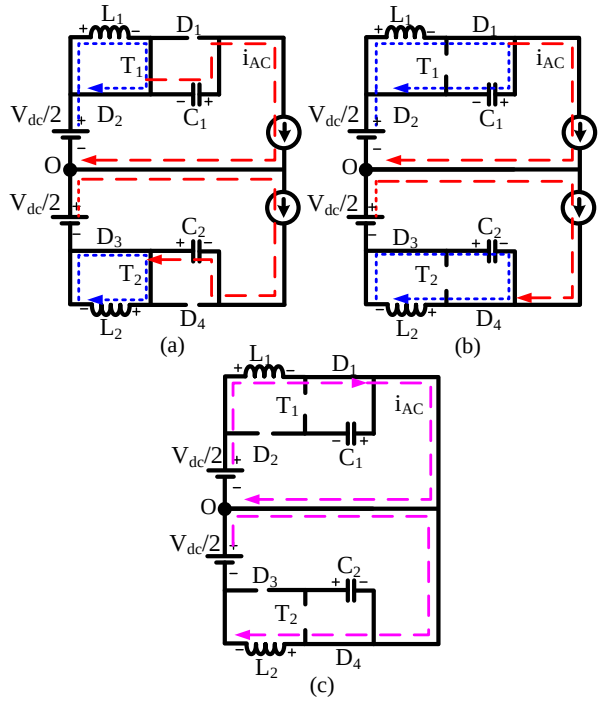

Fig.2 *Operating states of the three-level MqSBNPCI. (a) NST mode 1, (b) NST mode 2 and (c) ST mode.*

TABLE I
SWITCHING STATES OF THE PROPOSED INVERTER
(*X=A, B, C*)

Mode	Triggered Switches	ON Diodes	V_X
NST mode 1	T_1, T_2, S_{X1}, S_{X2}	D_2, D_3	$+V_{PN}/2$
	T_1, T_2, S_{X2}, S_{X3}		0
	T_1, T_2, S_{X3}, S_{X4}		$-V_{PN}/2$
NST mode 2	S_{X1}, S_{X2}	D_1, D_2, D_3, D_4	$+V_{PN}/2$
	S_{X2}, S_{X3}		0
	S_{X3}, S_{X4}		$-V_{PN}$
ST	S_{X1}, S_{X2}, S_{X3}, S_{X4}	D_1, D_4	0

In this paper, a combination of the modified qSB (MqSB) network with a three-level neutral point clamped (NPC) inverter is introduced. A third harmonic injection method and modified phase-shift (PS) carrier control method is considered to control the introduced topology to obtain high voltage gain with low voltage stress on capacitors and diodes as well as high modulation index. The output voltage is also regulated by applying a PI controller. The simulation and experimental results are shown to validate the effectiveness of the proposed structure.

2. Main content

2.1. Three-level quasi-switched boost NPC inverter topology

As illustrated in Fig. 1, the introduced topology consists of the MqSB network which is formed by two identical impedance networks including two inductors (L_1, L_2), two capacitors (C_1, C_2), four diodes (D_1, D_2, D_3, D_4), two active switches (T_1, T_2) and the traditional NPC structure.

2.1.1 Operation principles

Similar to other single-stage inverters, this structure also operates under two main modes: non-shoot-through (NST) mode and shoot-through (ST) mode. In NST mode, the inverter is able to produce three-level voltage at the output terminal by triggering corresponding switches. To simply, in non-ST modes, the inverter side is considered as a current source, I_{AC} as shown in Table I. When S_{X1} and S_{X2} are switched "ON", the output of the inverter is achieved $+V_{PN}/2$, where V_{PN} is the DC-link voltage generated by the MqSB network. While the output voltage obtains $-V_{PN}/2$ when S_{X3} and S_{X4} are turned "ON". The zero value is produced at output voltage when S_{X2} and S_{X3} are triggered "ON". The NST mode consists of two sub-mode which are NST mode 1 and NST mode 2, as presented in Table I. The ST mode is achieved when all switches of inverter leg are triggered "ON", simultaneously. As a result, the output load voltage in this time interval is zero. Therefore, the ST state is generated in the zero vector in order not to cause the distortion at output voltage.

2.1.1.1 NST mode

In NST mode 1, the switches T_1 and T_2 are turned on, as shown in Fig. 2(a). The diodes D_1 and D_4 are reverse-biased, while the diodes D_2 and D_3 are forward-biased. The inductor L_1 and L_2 currents are kept constant. The voltage across inductors L_1 and L_2 are obtained as following equations:

$$V_{L1} = L_1 \frac{di_{L1}}{dt} = 0 \tag{1}$$

$$V_{L2} = L_2 \frac{di_{L2}}{dt} = 0 \tag{2}$$

Similarly, the current through the capacitors C_1 and C_2 are expressed as:

$$C_1 \frac{dv_{C1}}{dt} = -i_{AC} \tag{3}$$

$$C_2 \frac{dv_{C2}}{dt} = -i_{AC} \tag{4}$$

In NST mode 2, the switches T_1 and T_2 are turned off, as shown in Fig. 2(b). The diodes D_1, D_2, D_3, and D_4 are

forward-biased. The capacitors C_1 and C_2 are charged from L_1 and L_2. The voltage across inductors L_1 and L_2 are obtained as:

$$L_1 \frac{di_{L1}}{dt} = -V_{C1} \tag{5}$$

$$L_2 \frac{di_{L2}}{dt} = -V_{C2} \tag{6}$$

Similarly, the current through the capacitors C_1 and C_2 are calculated as:

$$C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{AC} \tag{7}$$

$$C_2 \frac{dv_{C2}}{dt} = i_{L2} - i_{AC} \tag{8}$$

2.1.1.2 ST Mode

During the ST mode, the switches S_{X1} to S_{X4} of the NPC inverter are turned on at the same time, while the switches T_1 and T_2 are turned off, simultaneously. The equivalent circuit for this mode is shown in Fig. 2(c). The diodes D_1 and D_4 are forward-biased, while the diodes D_2 and D_3 are reverse-biased. The inductors L_1 and L_2 are stored energy from the input power source. The voltage across inductors L_1 and L_2 are obtained as:

$$L_1 \frac{di_{L1}}{dt} = \frac{V_{dc}}{2} \tag{9}$$

$$L_2 \frac{di_{L2}}{dt} = \frac{V_{dc}}{2} \tag{10}$$

Similarly, the current through the capacitors C_1 and C_2 are found as:

$$C_1 \frac{dv_{C1}}{dt} = 0 \tag{11}$$

$$C_2 \frac{dv_{C2}}{dt} = 0 \tag{12}$$

2.1.2 Third harmonic injection control method

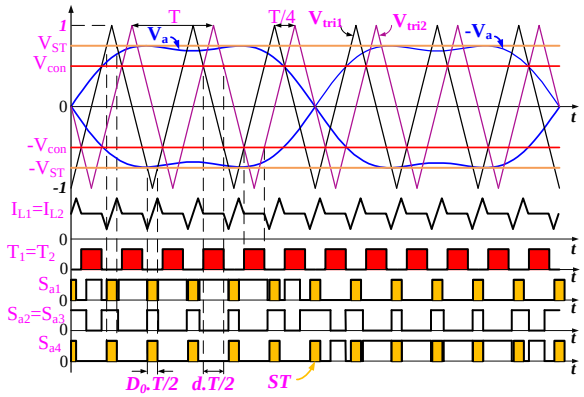

Fig. 3 *PWM control strategy for the three-level MqSBNPCI for the phase-A switch.*

With the operating principle of 3L-MqSBNPCI mentioned above, the active switches of the MqSB network are turned on when the ST signal of the 3L-NPCI circuit is zero. Moreover, the switches T_1 and T_2 should be triggered off when the ST control signal of the inverter leg is generated. Fig. 3 shows the PWM strategy for 3L-MqSBNPCI based on the third harmonic injection scheme. Similar to the conventional PWM strategy based on a phase-shift technique for 3L-NPCI, this control method also uses two reference waveforms (V_x and $-V_x$, $x=a, b, c$) with one carrier (V_{tri1}) to generate a three-level voltage at output pole voltage, as illustrated in Fig. 3. This carrier waveform is combined with V_{ST} and $-V_{ST}$ to create the ST signal of the inverter leg. Whereas, the control signals of two switches of the MqSB network are generated by using V_{tri2} compared with two control signals V_{con} and $-V_{con}$.

The three-phase reference signals are defined as:

$$\begin{cases} V_a = 2/\sqrt{3} m \sin(\theta) + \frac{1}{6} \times \frac{2}{\sqrt{3}} m \sin(3\theta) \\ V_b = 2/\sqrt{3} m \sin(\theta + 2\pi/3) + \frac{1}{6} \times \frac{2}{\sqrt{3}} m \sin(3\theta) \\ V_c = 2/\sqrt{3} m \sin(\theta - 2\pi/3) + \frac{1}{6} \times \frac{2}{\sqrt{3}} m \sin(3\theta) \end{cases} \tag{13}$$

where m is the modulation index, and V_a, V_b, V_c are the three-phase reference signals

2.1.3 Steady-State Analysis for the Three-Level MqSBNPCI

In one period of switching (T), the time interval of ST state is $D_0.T$, while $d.T$ is the time interval of NST mode 1. Therefore, the value $(1\text{-}D_0\text{-}d).T$ is the time interval of NST mode 2. Applying the volt-second balance for two inductors L_1 and L_2 with the note that $(V_{C1}=V_{C2}=V_C)$, the voltage across these capacitors and can be calculated as:

$$V_{C1} = V_{C2} = \frac{D_0}{2(1 - D_0 - d)} V_{dc} \tag{14}$$

Applying charge-second balance in steady-state equilibrium across the capacitors C_1 and C_2 are found as:

$$I_{L1} = I_{L2} = \frac{(1 - D_0)}{(1 - D_0 - d)} i_{AC} \tag{15}$$

where D_0 is ST duty ratio, d is duty cycle of T_1 and T_2. i_{AC} is the equivalent output current.

The peak value of DC-link voltage (V_{PN}) is identified as:

$$V_{PN} = V_{dc} + 2.V_C = \frac{1 - d}{1 - D_0 - d} V_{dc} \tag{17}$$

The peak value of output phase voltage is identified as:

$$V_{x,peak} = m.\frac{2}{\sqrt{3}}.\frac{V_{PN}}{2} = \frac{m}{\sqrt{3}}.\frac{1 - d}{1 - D_0 - d} V_{dc} \tag{18}$$

The boost factor of inverter is calculated as:

$$B = \frac{V_{PN}}{V_{dc}} = \frac{1 - d}{1 - D_0 - d}. \tag{19}$$

The voltage gain (G) of the inverter is expressed as:

$$G = \frac{V_{x,peak}}{V_{dc}} = \frac{m}{\sqrt{3}}.\frac{1 - d}{1 - D_0 - d} \tag{20}$$

The relationship between modulation index, the ST duty ratio, and the duty cycle of MqSB's switches are presented as:

$$\begin{cases} m + D_0 \le 1 \\ D_0 + d < 1 \end{cases} \quad (21)$$

2.1.4 Parameter selection

The inductor current ripple and capacitor voltage ripple is calculated based on equations (9) – (12) as equation (22). Noted that the inductor L_1 and L_2 are considered as $L_1 = L_2 = L$, and capacitor C_1 and C_2 are considered as $C_1 = C_2 = C$.

$$\begin{cases} \Delta I_L = \dfrac{1}{4L} V_{dc} D_0 T \\ \Delta V_C = \dfrac{1}{2C} i_{AC} dT \end{cases} \quad (22)$$

where ΔI_L and ΔV_C are inductor current ripple and capacitor voltage ripple, respectively.

The inductor and capacitor are selected in term of $\Delta I_L \le \%x.I_L$, and $\Delta V_C \le \%y.V_C$, where $\%x$ and $\%y$ are maximum percentages of inductor current ripple and capacitor voltage ripple. Thus, the inductor and capacitor are calculated as:

$$\begin{cases} L_1 = L_2 \ge \dfrac{D_0(1-D_0-d)T \cdot V_{dc}}{4\%x(1-D_0)i_{AC}} \\ C_1 = C_2 \ge \dfrac{d(1-D_0-d)T \cdot i_{AC}}{2\%yD_0V_{dc}} \end{cases} \quad (23)$$

The maximum inductor current is Selected as:

$$I_{L\max} = I_L + \frac{\Delta I_L}{2} = \frac{1-D_0}{1-D_0-d} I_{AC} + \frac{1}{8L} V_{dc} D_0 T \quad (24)$$

The maximum capacitor voltage is expressed in equation (14).

The switches and diodes of quasi-switched boost network (T_1, T_2, D_1, D_2, D_3, D_4) are selected in term of that the voltage stress of these devices is equal to capacitor voltage and current stress of these devices is equal to maximum inductor current.

2.1.5 Overall of output voltage regulation

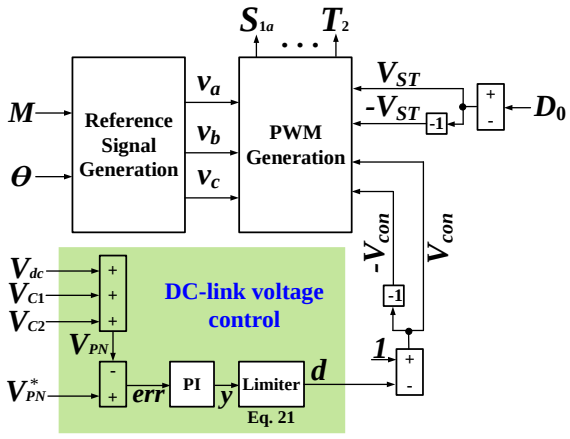

Fig. 4. *Output voltage control block.*

As shown in equation (18), the output voltage can be regulated through modulation index m and DC-link voltage. In this work, the modulation index is fixed, and the DC-link voltage is controlled to obtain the desired output voltage. To do that, the input voltage and capacitor voltages are measured to calculate the actual DC-link voltage. The error between the desired DC-link voltage and actual DC-link voltage feeds to PI controller to calculate the coefficient d. Noted that, only coefficient d is adopted to regulate the DC-link voltage. The ST duty ratio D_0 is kept constant in this work. When the DC-link voltage is regulated, the output load voltage is achieved the desired value with a very mall error [13]. The overall of output voltage control is shown in Fig. 4.

2.1.6 The comparison to other configurations.

Fig. 5 shows the investigations about the voltage gain versus modulation index for this topology and PWM method, and it is noted that the modulation index is set to $(1 - D_0)$ to achieve the highest voltage gain. As presented in Fig. 5, the voltage gain of the 3L-MqSBNPCI depends on the boost factor in (19) while the boost factor based on two coefficients which are the duty cycle of the MqSB network's active switches d and the ST duty ratio D_0. With the increase of d, the boost factor of the 3L-MqSBNPCI is increased, whereas the boost factor of other topologies is just up to the D_0. When the d value is 0.5, the 3L-MqSBNPCI produces a similar boost factor to the other configurations. However, by applying the third harmonic injection method, the qZSNPCI in [7] and the 3L-MqSBNPCI has the larger voltage gain which is $2/\sqrt{3}$ times larger than the others, as illustrated in Fig. 5. The 3L-MqSBNPCI just provides superior voltage gain when $d > 0.5$. For that reason, in this paper, the value 0.6 was selected for coefficient d as an example to analyze the effectiveness of the proposed topology.

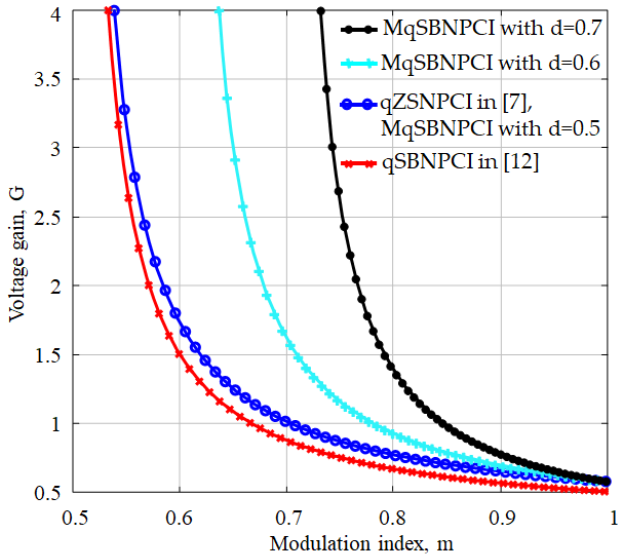

Fig. 5. *Investigation about voltage gain versus modulation index.*

Fig. 6 shows the investigations of voltage stress on power components such as diode voltage stress, capacitor voltage stress, and switch voltage stress. The proposed inverter is superior in diode voltage stress, capacitor voltage stress and switch voltage stress compare with [12]. The 3L-MqSBNPCI will reduce 30% voltage stress of D_1, D_4, C_1, C_2, T_1, and T_2 compare with [12] when voltage gain is 5.

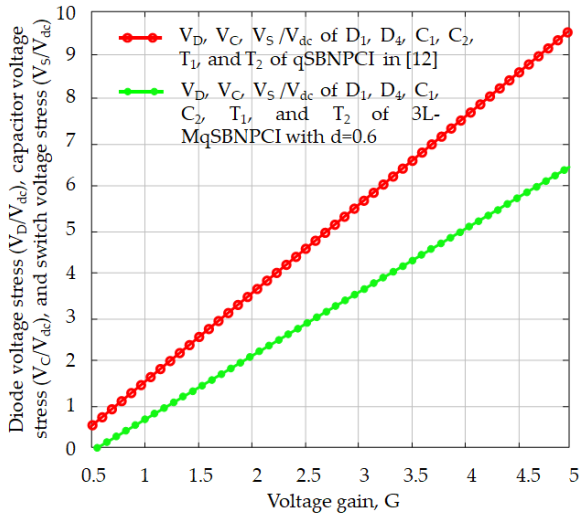

Fig. 6. *Investigation about diode voltage stress, capacitor voltage stress and switch voltage stress versus voltage gain.*

2.2. Simulation and Experimental Results

2.2.1 Simulation results

TABLE II
PARAMETERS USED IN SIMULATION AND EXPERIMENT

Parameter/Component		Attributes
Input voltage	V_{dc}	200 V
Desired output phase voltage	V_X	110 Vrms
Output frequency	f_o	50 Hz
Carrier frequency	f_s	5 kHz
ST duty ratio	D_0	0.15
ST duty ratio of the two switches T_1 and T_2	d	0.6
Modulation index	M	0.85
Boost inductor	$L_1 = L_2$	1 mH/ 20 A
Capacitors	$C_1 = C_2$	2200 µF/400 V
Three-phase LC filter	L_f and C_f	3 mH and 10 µF
Three-phase resistive load	R_{load}	40 Ω

The accuracy of the proposed inverter is validated by simulation results with the help of PSIM software. The parameters used for simulation are listed in Table II. Before feeding to three-phase resistor load, the three-phase low pass filter is used to mitigate the magnitude of high-frequency harmonics. By applying 3 mH and 10 µF for LC filter, the cut-off frequency of this filter is 1 kHz, approximately. The duty cycle of T_1 and T_2 is set to 0.6.

Fig. 7 shows the simulation results for input voltage, capacitor voltages, output pole voltage, output phase voltage, and harmonic spectrum. By using 0.6 for *d* and 0.15 for ST duty ratio D_0, as shown in Table II, the voltages of capacitors C_1 and C_2 are boosted to 60 V from 200V of the DC input source, as illustrated in Fig. 7. Therefore, the peak value of DC-link voltage can be identified as 320 V by summing the capacitor voltages and the input voltage. The peak-peak value of output pole voltage is the DC-link voltage which has three-level: 160 V ($+V_{PN}/2$), 0 V, and -160 V ($-V_{PN}/2$). The output phase voltage has seven-level and its peak-peak values are varied from $-2/3V_{PN}$ to $+2/3V_{PN}$, as shown in Fig. 7. By using 0.85 for the modulation index, the peak value of output load voltage is 156 V, approximately. The THD value of output phase voltage is 55.3%, which is measured by using the harmonic spectrum in Fig.7.

Fig. 8 shows the simulation results for DC-link voltage, line-line voltage. By using the full ST insertion, the DC-link voltage is varied from zero to the peak-value of DC-link voltage which is 320 V achieved in NST mode. The peak value of output line-line voltage is equal to DC-link voltage, so the top part of V_{AB} is varied from zero to 320 V, as illustrated in Fig. 8.

Fig. 9 shows the simulation results of the inductor currents, three-phase output load voltage, and three-phase output load current. The currents on inductors L_1 and L_2 are equal to each other. The average value of inductor currents is found to be 12.2 A and 12.1 A for I_{L1} and I_{L2}, respectively. Because of applying the low-pass filter before the resistor load, the output load voltage, as well as the output load current, have good quality. The RMS value of output load voltage and output load current are measured as 110 V_{RMS} and 2.8 A_{RMS}.

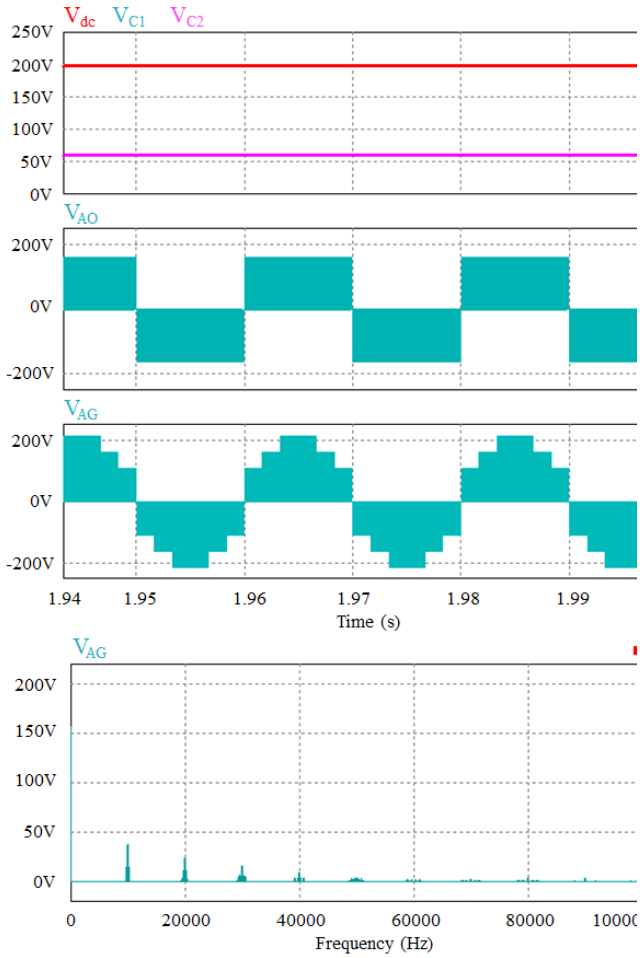

Fig. 7. *Simulation results of input voltage (V_{dc}), capacitor voltages (V_{C1}, V_{C2}), output pole voltage (V_{AO}), output phase voltage (V_{AG}), the harmonic spectrum for V_{AG}.*

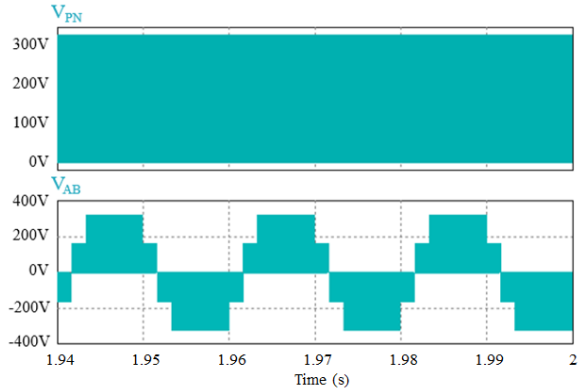

Fig. 8. *Simulation results of dc-link voltage (V_{PN}), line-line voltage (VAB), common-mode voltage (CMV).*

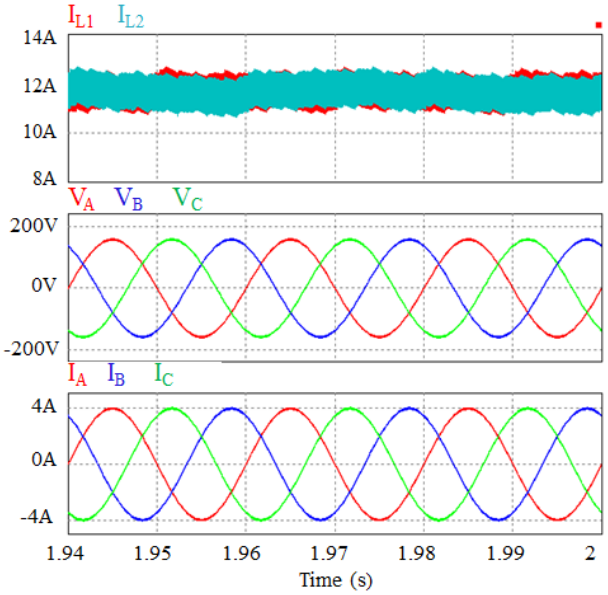

Fig. 9. *Simulation results of inductor current (I_{L1}, I_{L2}), three-phase output load voltage (V_A, V_B, V_C), three-phase output load*

Fig. 10 shows the simulation results of DC-link voltage, inductor current, active switch voltage stress, diode voltage stress. The inductor L_1 stores energy in ST mode which appeared when the diode D_2 is reserved bias, as illustrated in Fig. 10. In this time interval, the current through L_1 is linearly increased.

The inductor current ripple is measured as 1.44 A for L_1. The inductor current is kept constant when T_1 is turned on and the diode D_1 is reserved bias. As all switches of the inverter branch are triggered on, the DC-link voltage is zero in ST mode, whereas it achieves maximum value in NST mode, as presented in Fig. 10.

The conduction loss of semiconductor devices of quasi-switched boost network has been measured with the help of PSIM software. The result is shown in Figure 11.

2.2.2 Experimental results

A 1 kW prototype based on the DSP TMS320F28335 microcontroller is built in the laboratory to verify the effectiveness of the three-level MqSBNPCI with the proposed PWM control strategy. Fig. 12 shows a photograph of the laboratory prototype. The prototype uses the same parameters as those in the simulation in Table II. The input voltage is 200 V. The desired RMS output load voltage is 110 V. The output frequency is 50 Hz. The switching frequency of the MqSBNPC inverter circuit is 5 kHz. All FGL40N150D IGBTs in the prototype are controlled by TLP250 amplifiers. The four power diodes are DSEI60-12A. The boost inductors L_1 = L_2 are 1mH/20A. The two capacitors C_1 and C_2 are 2200 µF/400 V. The output voltage is filtered by a three-phase low-pass filter. The modulation index and ST duty cycle in the proposed PWM control strategy are 0.85 and 0.15, respectively.

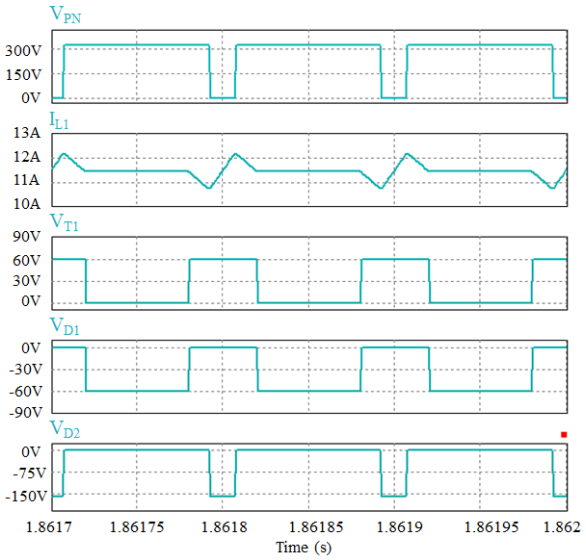

Fig. 10. *Simulation results of dc-link voltage (V_{PN}), inductor current (I_{L1}), MqSB network's active switch voltage stress (V_{T1}), Diode voltage stress (V_{D1}, V_{D2}).*

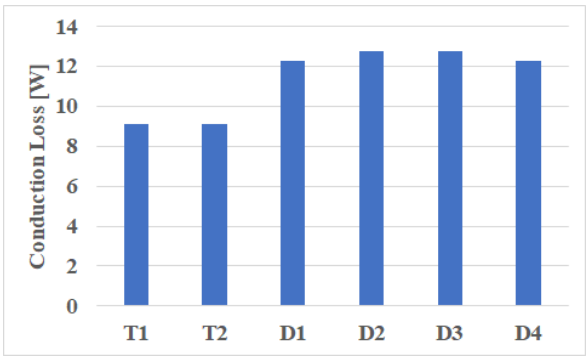

Fig. 11. *Conduction loss of semiconductor devices of quasi-switched boost network.*

Fig. 13 shows the experimental results of the three-level MqSBNPCI with the proposed PWM control method when V_{dc} = 200 V and d = 0.6. The voltages of the capacitors C_1 and C_2 are boosted to 52 V, respectively, from the 200 V input voltage. The measured peak value of the DC-link voltage is 305 V, as presented in Fig. 13(c). The waveforms of output load voltage and output load current are sinewaves which are achieved by applying LC filter before feeding to the load, as illustrated in Fig. 13(b). Their RMS values are 105 V_{RMS} and 2.55 A_{RMS}, respectively.

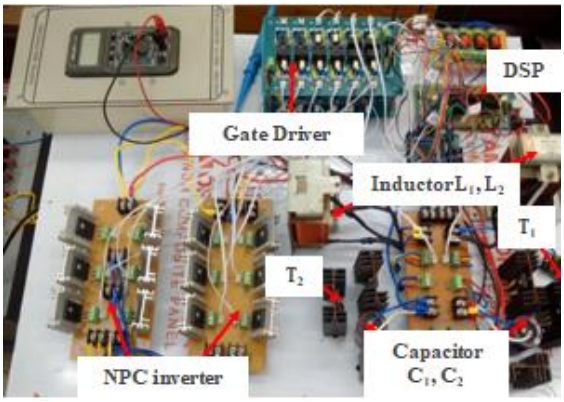

Fig. 12. *A laboratory prototype of the three-level MqSBNPCI.*

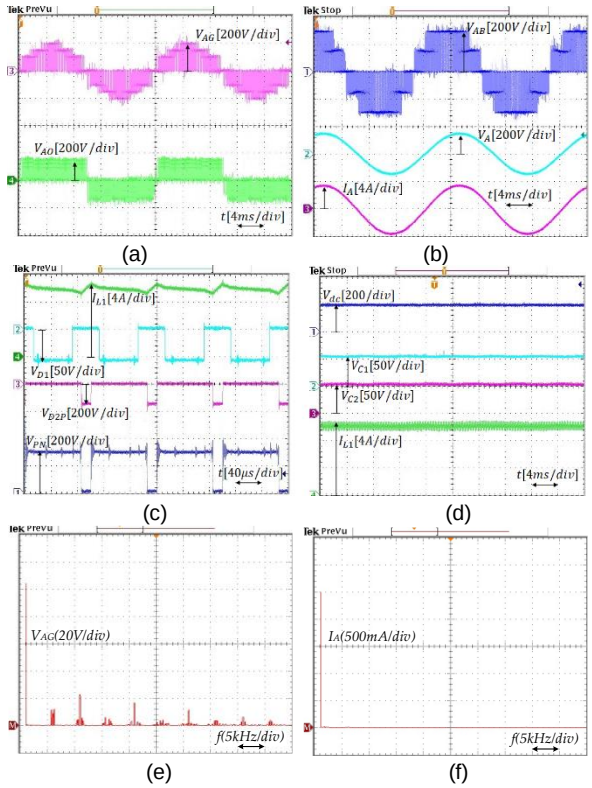

Fig. 13. *Experimental results for the three-level MqSBNPCI when V_{dc} = 200 V and d = 0.6.*

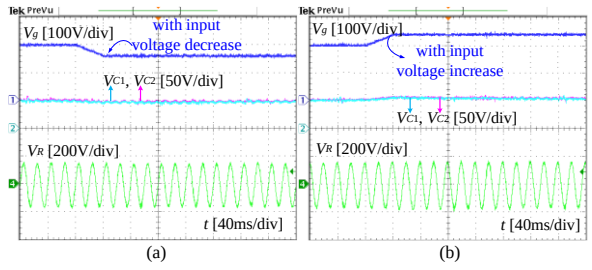

Fig. 14. *Experimental results for DC-link voltage control and output load voltage control. (a) input voltage decrement, (b)input voltage increment.*

While, when not applying the thrid harmonic injection, the modulation index m, ST duty ratio D_0 and coefficient d are calculated as 0.8069, 0.1931 and 0.6 to generate 110 V_{RMS} at output voltage. The capacitor voltage is boosted to 93 V. It can be seen that the third harmonic injection can reduce the voltage stress of devices significantly. The pole voltage has three levels: -153 V, 0, +153 V. The harmonic spectrum of V_{AG} and I_A are shown in Fig. 13(e) and 13(f). It can be seen that the peak-value of harmonic spectrum of output phase voltage is achieved at first-order harmonic (50Hz), which is 105V, which equals to the RMS value of output load voltage. The magnitude of the first harmonic of I_A equals to RMS value of output load current which is 2.55, approximately. Based on the harmonic spectrum of output voltage and current in Fig. 13(e) and (f), the THD values of these waveforms can be calculated as 64.5% and 3.92% compare to first-order harmonic.

The DC-link voltage control and output load voltage control are also implemented in two cases: 1) the DC input source decreases from 200 V to 160 V, and 2) the DC input power source increases from 200 V to 240 V. In both cases, the voltages on capacitors V_{C1} and V_{C2} are maintained as 60 V with a very small difference between them. The output load voltage is kept at 110 V_{RMS} without the variation of DC input power supply.

3. Conclusions

A novel three-level MqSBNPCI and its PWM control strategy are proposed in this paper. The main features of the three-level MqSBNPCI with the proposed PWM technique are as follows: 1) enhanced modulation index, 2) improved the voltage gain, and 3) reduced the voltage stress on power components. The circuit analysis, operating principles, and simulation results of the proposed three-level MqSBNPCI are presented. A laboratory prototype has been constructed to verify the operating principle of the proposed inverter. Simulations and experimental results confirmed the accuracy of the theoretical analysis. The proposed three-level MqSBNPCI is suitable for high-power and medium-power applications such as photovoltaic systems, fuel cells, motor drives, etc.

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